RAMAIAH
Institute of Technology

CURRICULUM

for the batch 2018 – 2020

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

M. TECH (VLSI DESIGN AND EMBEDDED SYSTEMS)

I – IV Semester

RAMAIAH INSTITUTE OF TECHNOLOGY

(Autonomous Institute, Affiliated to VTU)

BANGALORE – 560 054

About the Institute

Ramaiah Institute of Technology (RIT) (formerly known as M. S. Ramaiah Institute of Technology) is a self-financing institution established in Bangalore in the year 1962 by the industrialist and philanthropist, Late Dr. M S Ramaiah. The institute is accredited with A grade by NAAC in 2016 and all engineering departments offering bachelor degree programs have been accredited by NBA. RIT is one of the few institutes with prescribed faculty student ratio and achieves excellent academic results. The institute was a participant of the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. All the departments have competent faculty, with 100% of them being postgraduates or doctorates. Some of the distinguished features of RIT are: State of the art laboratories, individual computing facility to all faculty members. All research departments are active with sponsored projects and more than 140 scholars are pursuing PhD. The Centre for Advanced Training and Continuing Education (CATCE), and Entrepreneurship Development Cell (EDC) have been set up on campus. RIT has a strong Placement and Training department with a committed team, a good Mentoring/Proctorial system, a fully equipped Sports department, large airconditioned library with over 1,00,000 books with subscription to more than 300 International and National Journals. The Digital Library subscribes to several online e-journals like IEEE, JET etc. RIT is a member of DELNET, and AICTE INDEST Consortium. RIT has a modern auditorium, several hi-tech conference halls and all are air-conditioned with video conferencing facilities. It has excellent hostel facilities for boys and girls. RIT Alumni have distinguished themselves by occupying high positions in India and abroad and are in touch with the institute through an active Alumni Association. RIT obtained Academic Autonomy for all its UG and PG programs in the year 2007. As per the National Institutional Ranking Framework, MHRD, Government of India, Ramaiah Institute of Technology has achieved 60^{th} rank in 2018 among the top 100 engineering colleges across India.

About the Department

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a research center under VTU. The department currently offers a B. E. program with an intake of 120, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DST, VTU, VGST and AICTE with funding amount worth Rs. 1 crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.

Vision of the Institute

To be an Institution of International Eminence, renowned for imparting quality technical education, cutting edge research and innovation to meet global socio economic needs

Mission of the Institute

MSRIT shall meet the global socio-economic needs through

- *Imparting quality technical education by nurturing a conducive learning environment through continuous improvement and customization*
- *Establishing research clusters in emerging areas in collaboration with globally reputed organizations*
- *Establishing innovative skills development, techno-entrepreneurial activities and consultancy* for socio-economic needs

Quality Policy

We at M. S. Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established Quality Management System complemented by the synergistic interaction of the stake holders concerned

Vision of the Department

To be, and be recognized as, an excellent Department in Electronics & Communication Engineering that provides a great learning experience and to be a part of an outstanding community with admirable environment.

Mission of the Department

To provide a student centered learning environment which emphasizes close faculty-student interaction and co-operative education.

To prepare graduates who excel in the engineering profession, qualified to pursue advanced degrees, and possess the technical knowledge, critical thinking skills, creativity, and ethical values.

To train the graduates for attaining leadership in developing and applying technology for the betterment of society and sustaining the world environment

Program Educational Objectives (PEOs)

PEO1: *Be successful practicing professionals or pursue doctoral studies in areas related to the program, contributing significantly to research and development activities*

PEO2: *Engage in professional development in their chosen area by adapting to new technology and career challenges*

PEO3: *Demonstrate professional, ethical, and social responsibilities of the engineering profession*

Program Outcomes (POs)

PO1: ***Development of Solutions:*** *An ability to independently carry out research/investigation and development work to solve practical problems*

PO2: ***Technical Presentation Skills:*** *An ability to write and present a substantial technical report/document*

PO3: ***Analyze Complex Systems:*** *A practical ability and theoretical knowledge to design and analyze VLSI and embedded systems*

PO4: ***Develop Novel Designs:*** *An ability to apply their in-depth knowledge in VLSI and emdedded systems domain to evaluate, analyze and synthesize existing and novel designs*

PO5: ***Team Work and Project Management:*** *An ability to effectively participate as a team member and develop project management skills necessary for a professional environment*

CURRICULUM COURSE CREDITS DISTRIBUTION

Semester	Professional Courses – Core (Theory & Lab) (PC-C)	Professional Courses – Electives (PC-E)	Technical Seminar (TS)	Project Work/Internship (PW/IN)	Credits in a semester
First	10	12	2		**24**
Second	10	12	2		**24**
Third	4	4		10	**18**
Fourth				22	**22**
Total	**24**	**28**	**4**	**32**	**88**

SCHEME OF TEACHING M. Tech (VLSI Design and Embedded Systems)

(Batch 2018 – 2020)

I SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE11	Advanced Engineering Mathematics	PS-C	3	1	0	4	5
2.	MVE12	CMOS VLSI Circuits	PS-C	4	0	0	4	4
3.	MVEExx	Elective 1	PS-E	4	0	0	4	4
4.	MVEExx	Elective 2	PS-E	4	0	0	4	4
5.	MVEExx	Elective 3	PS-E	4	0	0	4	4
6.	MVEL13	Digital System Design Laboratory	PS-C	0	0	1	1	2
7.	MVEL14	Advanced Embedded Systems Laboratory	PS-C	0	0	1	1	2
8.	MVE15	Technical Seminar I	TS	0	0	2	2	4
			Total	**19**	**1**	**4**	**24**	**29**

II SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE21	VLSI System Design	PS-C	3	1	0	4	5
2.	MVE22	Analog and Mixed Mode IC Design	PS-C	4	0	0	4	4
3.	MVEExx	Elective 4	PS-E	4	0	0	4	4
4.	MVEExx	Elective 5	PS-E	4	0	0	4	4
5.	MVEExx	Elective 6	PS-E	4	0	0	4	4
6.	MVEL23	Analog and Mixed Mode IC Design Laboratory	PS-C	0	0	1	1	2
7.	MVEL24	Advanced Microcontroller Laboratory	PS-C	0	0	1	1	2
8.	MVE25	Technical Seminar II	TS	0	0	2	2	4
			Total	**19**	**1**	**4**	**24**	**29**

III SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE31	Low Power VLSI Design	PC-C	4	0	0	4	4
2.	MVEExx	Elective 7	PC-E	4	0	0	4	4
3.	MVE32	Internship/Industrial Training	IN	0	0	4	4	8
4.	MVE33	Project Work – I	PW	0	0	6	6	12
			Total	**8**	**0**	**10**	**18**	**28**

IV SEMESTER

Sl. No.	Course Code	Course Title	Category	Credits				Contact Hours
				L	T	P	Total	
1.	MVE41	Project Work – II	PW	0	0	22	22	44
			Total	**0**	**0**	**22**	**22**	**44**

LIST OF ELECTIVES

SI. No.	Course Code	Subject	Credits				
			L	T	P	SS	Total
1.	MVEE01	Advanced Embedded Systems	4	0	0	0	4
2.	MVEE02	Digital System Design using HDL	4	0	0	0	4
3.	MVEE03	Digital VLSI Testing	4	0	0	0	4
4.	MVEE04	Advanced Microcontrollers	4	0	0	0	4
5.	MVEE05	Advanced Digital Logic Verification	4	0	0	0	4
6.	MVEE06	MEMS and Nanoelectronics	4	0	0	0	4
7.	MVEE07	Internet of Things (IoT)	4	0	0	0	4
8.	MVEE08	Physics of Semiconductor Devices	4	0	0	0	4
9.	MVEE09	Synthesis and Optimization of Digital Circuits	4	0	0	0	4
10.	MVEE10	ASIC Design	4	0	0	0	4
11.	MVEE11	System on Chip Design	4	0	0	0	4
12.	MVEE12	Physical VLSI Design	4	0	0	0	4
13.	MVEE13	Advanced Computer Architecture	4	0	0	0	4
14.	MVEE14	VLSI Signal Processing	4	0	0	0	4
15.	MVEE15	Memory Technologies	4	0	0	0	4
16.	MVEE16	Communication Busses and Interfaces	4	0	0	0	4

ADVANCED ENGINEERING MATHEMATICS

Course Code: MVE11 **Credits: 3:1:0**

Prerequisites: Engineering Mathematics **Contact Hours: 70**

Course Coordinator: Sadashiva V Chakrasali

UNIT – I

Solving Linear Equations: Introduction, geometry of linear equations, Solution sets of linear systems, Gaussian elimination, matrix notation, inverses, Partitioned matrices, matrix factorization and determinants

Vector Spaces: Vector spaces and subspaces, linear independence, rank, basis and dimension, linear transformation, change of basis

UNIT – II

Graph Theory: Introduction, Isomorphism, Connected Graphs, Disconnected Graphs, Trees, Cut-sets, Vectors Spaces of Graphs, Electrical network analysis by graph theory

UNIT – III

Linear Differential Equations: Definitions, complete solutions, rules for finding the complementary function, inverse operator, rules for finding the particular integral, Cauchy's and Legendre's linear equations, linear dependence of solutions, simultaneous linear equations with constant coefficients

UNIT – IV

Partial Differential Equations: Introduction, formation of partial differential equations, solutions of partial differential equations, homogeneous linear equations with constant coefficients, working procedure to solve homogeneous linear equations, rules for finding complementary function, non-homogeneous linear equations

UNIT – V

Numerical Solution of Ordinary Differential Equations: Introduction, Taylor's series method, Euler's method, Runge – Kutta method, simultaneous first and second order differential equations, boundary value problems

References:

1. B. S. Grewal, "Higher Engineering Mathematics", 40th Edition, Khanna Publishers, 2010.
2. Strang. G, "Linear Algebra and its Applications", 4th Edition, Cengage Learning, 2014.
3. David C. Lay, "Linear Algebra and its Applications", 3rd Edition, Pearson Education, 2013.

4. Narsingh Deo, “Graph Theory with Applications to Engineering and Computer Science”, PHI learning, 2011.
5. N. Balabanian and T. A. Bickart, “Electrical Network Theory”, John Wiley and Sons, Inc, 1969.

Course Outcomes:

1. Employ linear system concepts in VLSI circuit design (POs: 1, 3, 4)
2. Analyze electronic circuits using graph theory techniques (POs: 1, 3, 4)
3. Model and analyze electronic circuits using integro differential equations (POs: 1, 3, 4)
4. Model and analyze electronic circuits using partial differential equations (POs: 1, 3, 4)
5. Employ numerical solution of ordinary differential equations in various electronic circuit design and analysis (POs: 1, 3, 4)

CMOS VLSI CIRCUITS

Course Code: MVE12 **Credits: 4:0:0**

Pre requisites: Digital Design **Contact Hours: 56**

Course Coordinator: M. Nagabushanam

UNIT – I

MOS Transistor Theory: n MOS/p MOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter.

UNIT – II

CMOS Process Technology: Semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD, refractory gate, multilayer inter connect), Circuit elements, resistor, capacitor, interconnects, sheet resistance & standard unit of capacitance concepts delay unit time, inverter delays, driving capacitive loads, RC delay Line, Super Buffers, propagation delays, MOS mask layout, stick diagram, design rules and layout, symbolic diagram, masking, scaling of MOS circuits.

UNIT – III

Basics of Digital CMOS Design: Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits- Introduction, Behavior of Bi-stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Dynamic CMOS circuit techniques.

UNIT – IV

Dynamic CMOS and clocking: Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking- clock generation, clock distribution, clocked storage elements

UNIT – V

Circuit Simulation: Introduction to circuit simulation, Spice tutorials, Device models, Device characterization, circuit characterization, Simulation mismatches, Monte Carlo simulation

References:

1. Neil H E Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design: A System Perspective", 3rd Edition, Pearson Education, 2006.
2. Wayne Wolf, "Modern VLSI Design: System on Silicon", 3rd Edition, PHI, 2008.
3. Douglas A Pucknell, Kamran Eshraghian, "Basic VLSI Design", PHI, 3rd Edition, 2009.
4. Sung Mo Kang, Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hill, 3rd Edition, 2003.

Course Outcomes:

1. Describe basics of CMOS digital integrated circuits. (POs: 3, 4)
2. Discuss the fabrication process in CMOS technologies. (POs: 1, 3, 4)
3. Analyze the switching characteristics of VLSI circuits. (POs: 1, 3, 4)
4. Design and analyze dynamic CMOS circuits. (POs: 1, 3, 4)
5. Describe the circuit simulation process for VLSI circuits. (POs: 1, 3, 4)

DIGITAL SYSTEM DESIGN LABORATORY

Course Code: MVEL13 **Credits: 0:0:1**

Prerequisites: Digital Electronics **Contact Hours: 28**

Course Coordinator: Gangadharaiah S L

LIST OF EXPERIMENTS

Using Verilog code design, simulate and synthesize the following with a suitable FPGA.

1. 8 to 3 programmable priority encoder
2. Full Adder using structural modeling
3. Flip Flops (D, SR, T, JK)
4. 3 bit arbitrary Counter, 4 bit binary up/down/up-down counter with synchronous reset, 4 bit Johnson counter, BCD counter
5. Sequential block to detect a sequence (say 11101) using appropriate FSM
6. 8 bit ripple carry adder and carry skip adder
7. 8 bit Carry Select Adder
8. 8 bit Serial, Parallel Multiplier and generate report on area and delay

Using System Verilog code, simulate the following

9. Full Subtractor using structural modeling
10. Flip Flops (D, SR, T, JK)
11. 3-bit synchronous counters, synchronous arbitrary counters
12. 4-bit asynchronous counters

References:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach using Verilog", Elsevier, 2010.
2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, 2nd Edition, 2010.
3. Stuart Sutherland, "RTL Modeling with System Verilog for Simulation and Synthesis: Using System Verilog for ASIC and FPGA Design", CreateSpace Independent Publishing Platform, First Edition, 2017.

Course Outcomes:

1. Design and model complex combinational circuits using HDL at behavioral, structural and RTL levels. (POs: 1, 3, 4, 5)
2. Design and model complex sequential circuits using HDL at behavioral, structural and RTL levels. (POs: 1, 3, 4, 5)
3. Develop the test benches to simulate combinational and sequential circuits. (POs: 1, 3, 4, 5)
4. Learn how the language infers hardware and helps to simulate and synthesize the digital system. (POs: 1, 3, 4, 5)
5. Implement and analyze the digital systems using FPGAs with respect to speed and area. (POs: 1, 3, 4, 5)

ADVANCED EMBEDDED SYSTEMS LABORATORY

Subject Code: MVEL14 **Credits: 0:0:1**

Prerequisites: Embedded Systems **Contact Hours: 28**

Course Coordinator: K. V. Suma

LIST OF EXPERIMENTS

Part A – PCB Designing

1. Generation of schematic – Opamp Circuit
2. Generation of layout – Opamp Circuit
3. Circuit Selection
4. Bill of Materials and Net list
5. Layouts and Routing of the Circuit
6. Gerber file Generation and Online viewer

Part B – Unified Modeling Language (UML)

7. Model the static aspects of the system using Use Case Diagram in UML
8. Model the static aspects of the system using
    a. Basic Class Diagram and generate code in UML
    b. Optimized Class Diagram and generate code in UML
9. Model the elevator system using sequence diagram in UML

Part C – RTOS programs

10. Program in C to create a process using fork( ) function call (forkdemo.c) and to simulate in Linux platform
11. Program in C to generate a signal when a delete key is pressed (signal) and to simulate in Linux platform

Reference:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M4", Newnes, (Elsevier), 3rd Edition, 2014.

Course Outcomes:

1. Generate the schematic, netlist, bill of materials and layout for PCB of a given circuit (POs: 3, 5)
2. Generate Gerber files for actual PCB fabrication (POs: 4, 5)
3. Generate UML static diagrams for a given embedded application (POs: 1, 3, 4, 5)
4. Generate UML dynamic diagrams for a given embedded application (POs: 1, 3, 4, 5)
5. Implement the basic concepts of RTOS such as threads & processes (POs: 4, 5)

TECHNICAL SEMINAR – I

Course Code: MVE15 **Credits: 0:0:2**

Prerequisites: Nil **Contact Hours: 56**

LIST OF ACTIVITIES

1. Seminar: Research Methods
2. Seminar: Technical Report Writing
3. Source/Ideas for a Research Problem
4. Choosing Research Papers
5. Reading Research Papers
6. Summarizing Research Papers: Written
7. Presenting Research: Oral
8. **REVIEW – I**
9. Critiquing: Oral & Written
10. Detailed analysis of Block Diagrams: Written
11. Detailed Analysis of Block Diagrams: Oral
12. Proposing Technical Solutions: Written
13. Proposing Technical Solutions: Oral
14. **REVIEW – II**

Course Outcomes:

1. Identify a technical problem by performing a comprehensive literature survey (POs: 1, 2, 3, 4, 5)
2. Compare different solution methods presented in the literature for the technical problem identified (POs: 1, 2, 3, 4, 5)
3. Predict the impact of various software tools and methods for the identified problem (POs: 1, 2, 3, 4, 5)
4. Display initial simulation results, showing replication of existing approaches for the identified problem (POs: 1, 2, 3, 4, 5)
5. Construct a technical block diagram that shows an optimized solution for the identified problem, with respect to existing literature (POs: 1, 2, 3, 4, 5)

EVALUATION RUBRICS

Criteria	Max Marks	Achievement Levels				CO Mapping
		Inadequate (0 – 33%)	**Developing (34 – 66%)**	**Proficient (67 – 100%)**	**Marks Awarded**	
Introduction to area	**10**	No information about the specific technical details in the chosen area.	Some information about the area, but no clarity in internal details.	Clear presentation of the technical details, internal working, and rationale of design choices.		**CO1, CO2**
Literature Survey	**10**	Very few quality sources pertinent to the chosen technical area. No recent articles used.	Ample sources from recent past, but not from quality sources or with zero or very few citations.	Ample sources from quality journals and conferences recently published, and having abundant citations.		**CO1, CO2**
Problem Statement	**10**	No clear problem identified in chosen area.	Identification of problem area, but no knowledge of underlying technical details.	Clear identification of problem area, along with parameters having an influence on the performance.		**CO3**
Reproduction of Existing Results	**10**	No simulation results shown.	Individual blocks simulated, but no comprehensive simulation.	Complete and consistent reproduction of existing results using appropriate software tools.		**CO4**
Research Questions	**10**	No hypothesis proposed.	Hypothesis is not sound/practical, and not backed by technical arguments.	Sound and practical hypothesis proposed, along with supporting technical/intuitive arguments.		**CO5**
				TOTAL MARKS AWARDED		

VLSI SYSTEM DESIGN

Course Code: MVE21 **Credits: 3:1:0**

Prerequisites: CMOS VLSI **Contact Hours: 70**

Course Coordinator: Raghuram S

UNIT – I

Design Methodology and Tools: Structured Design Strategies, Design Methods, VLSI Design Flows.

Coping with Interconnect: Capacitive, Resistive, and Inductive Parasitics, Advanced Interconnect Techniques, Perspective – NoC Design

UNIT – II

Circuit Characterization and Performance Estimation: Delay Estimation – transient response, RC delay model, Elmore delay model, Linear Delay Model, Sizing with the method of Logical Effort.

Combinational and Sequential Circuit Design: Static CMOS, CMOS circuit design families: CVSL, Dynamic logic, Pass transistor circuits, Sequential circuits: circuit design of latches and flip-flops.

UNIT – III

Data Path Sub System Design: Introduction, Addition – Carry look ahead, Carry Select, Tree Adders – Brent Kung, Kogge Stone, Sklansky, Analysis of delay with PG network diagrams for adders, Subtraction, Comparators, Counters, Boolean Logical Operations, Coding, Shifters.

UNIT – IV

Array Subsystem Design: SRAM, Special Purpose RAMs, DRAM, Read Only Memory, Content Addressable Memory, Programmable Logic Arrays.

Special Purpose Subsystems: Packaging, Power Distribution, Clock.

UNIT – V

Timing Issues in Digital Circuits: Timing Classification of Digital Systems, Synchronous Design – Timing Basics, Skew and Jitter, Clock Distribution, Latch Based Techniques, Self-timed circuits, Synchronization and Arbiters

References:

1. Neil H.E. Weste, David Harris, "CMOS VLSI Design", Pearson Education, 4th Edition, 2014.
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective", Pearson Education India, 2nd Edition, 2003.
3. Wayne Wolf, "Modern VLSI Design: System on Silicon", Prentice Hall PTR/Pearson Education, 2nd Edition, 1998.
4. D. A. Pucknell, "Basic VLSI Design", PHI Publications, 2005.

Course Outcomes:

1. Analyze the effects of interconnects on performance **(**POs: 1, 3, 4)
2. Employ different performance metrics to predict the performance of VLSI circuits **(**POs:1, 3, 4)
3. Apply digital design concepts to demonstrate different data path functions **(**POs: 1, 3, 4)
4. Explain the structure and operation of different memory elements and some special subsystems. **(**POs: 1, 3, 4)
5. Predict variations in clock signals, and design circuits to reduce effects of large clock distribution networks. (POs: 1, 3, 4)

ANALOG AND MIXED MODE IC DESIGN

Course Code: MVE22 **Credits: 4:0:0**

Prerequisites: Digital & Analog Circuits **Contact Hours: 56**

Course Coordinator: S. L. Gangadharaiah

UNIT – I

Single Stage Amplifier: CS stage with resistance load, diode connected load, current source load, active load, triode load, CS stage with source degeneration, source follower, common-gate stage, cascode stage, folded cascode.

UNIT – II

Frequency Response of CS Stage: General considerations, Miller effect, Association of poles with nodes, Frequency response of common source stage.

Differential Amplifiers and Current Mirrors: Basic differential pair, common mode response, differential pair with MOS loads, Gilbert cell, Basic current mirror, cascode current mirror.

UNIT – III

Operational Amplifiers: One stage opamp, Two stage opamp, Gain boosting,output swing calculations, Common Mode Feedback, input range, limitations, Slew rate, PSRR, Noise in opamp

Stability and frequency compensation: general considerations, multipole systems, phase margin, basic frequency compensation, compensation of two-stage op-amp.

UNIT – IV

Band gap references and Switched Capacitor Circuits: General considerations, supply independent biasing, Temperature independent biasing, PTAT current generation, Constant Gm biasing, sampling switches, Switched Capacitor Amplifiers.

UNIT – V

Data Converter Architecture: DAC and ADC specifications, Qualitative analysis of Resistor string DAC, R-2R Ladder networks, current steering DAC, Cyclic DAC, Pipe line DAC, Flash ADC, Pipeline ADC, Integrating ADC.

References:

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill 2nd Edition, 2018.
2. Douglas R Holberg, Phillip E Allen, "CMOS Analog Circuit Design", Oxford University Press, 2nd Edition, 2013.
3. R. Jacob Baker "CMOS: Circuit Design, Layout, Simulation", Wiley Publications, 2009.

4. Behzad Razavi, "Micro electronics", Tata McGraw-Hill, 1st Edition, 2001.

Course Outcomes:

1. Employ the concept of MOS devices in various MOS amplifier applications (POs: 1, 3, 4)
2. Apply the concept of differential amplifiers with MOS loads and the frequency response of one stage op amp (POs: 1, 3, 4)
3. Apply the concept to construct one,two stage op amp & analyze the frequency compensation, stability of opamps (POs: 1, 3, 4)
4. Illustrate the concept of band gap references and switched capacitor circuits (POs: 1, 3, 4)
5. Analyze different types of ADC & DAC architectures (POs: 1, 3, 4)

ANALOG AND MIXED MODE IC DESIGN LABORATORY

Course Code: MVEL23 **Credits: 0:0:1**

Prerequisites: Digital and Analog Circuits **Contact Hours: 28**

Course Coordinator: S.L. Gangadharaiah

LIST OF EXPERIMENTS

1. Design the following Analog circuits with the given specifications and complete the design flow as mentioned below:
    a. Draw the schematic and perform: DC Analysis, AC Analysis, Transient Analysis
    b. Draw the Layout, verify DRC and check for LVS
        (i) CMOS Inverter
        (ii) Common source Amplifier
        (iii) Common Drain Amplifier
        (iv) Common Gate Amplifier
        (v) Differential Amplifier
        (vi) single stage op-amp
        (vii) Two stage op-amp

2. Design the following Digital/ Mixed signal cicuits and verify the functionality
    (i) 3-8 decoder using MOS technology
    (ii) Two-input OR gate using digital two input NOR gate and analog inverter
    (iii) Two-input NOR gate using analog two input NOR gate and digital inverter
    (iv) Two-input XOR gate using digital two input XNOR gate and analog inverter
    (v) R-2R digital to analog converter

References:

1. Cadence Analog and Mixed Mode Lab Manual, Developed by University Support Team, Cadence, Bangalore, version 3.0, 2014.
2. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw-Hill, 2nd Edition, 2018.
3. Phillip E Allen, Douglas R Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2004.

Course Outcomes:

1. Apply DRC, LVS and different analysis for various single stage amplifiers (POs: 1, 3, 4, 5)
2. Design the differential amplifier and apply the different analysis, LVS and DRC (POs: 1, 3, 4, 5)
3. Apply DRC, LVS and different analysis for operational amplifiers (POs: 1, 3, 4, 5)
4. Design the DAC converter and measure different parameters (POs: 1, 3, 4, 5)
5. Apply mixed signal simulation to OR, NOR and XOR gate (POs: 1, 3, 4, 5)

ADVANCED MICROCONTROLLERS LABORATORY

Course Code: MVEL24 **Credits: 0:0:1**

Prerequisites: Microcontrollers **Contact Hours: 28**

Course Coordinator: K V Suma

LIST OF EXPERIMENTS

1. ARM Cortex M4 Assembly programs for data transfer, arithmetic and logic operations
2. C programs on ARM Cortex M4 board for sorting, code conversion and factorial
3. Interfacing programs for ARM Cortex M4 with
   - (i) Display (LCD & LED) modules
   - (ii) 16 channel 8 bit ADC
   - (iii) DC motor speed control and measurement
   - (iv) Generation of Sine and Square waveforms using Dual DAC
   - (v) Elevator
   - (vi) Calculator-type keyboard
   - (vii) Relay output
   - (viii) Real Time Clock
   - (ix) Stepper Motor
   - (x) Temperature sensor monitoring and control

References:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M4", Newnes, (Elsevier), 3rd Edition, 2014.

Course Outcomes:

1. Use simulation and emulation IDE (POs: 4, 5)
2. Write, compile and debug assembly language program and C programs for ARM Cortex M4 (POs: 1, 3, 5)
3. Write C language programs to interface display modules and data converters to ARM Cortex M4 microcontroller (POs: 1, 4, 5)
4. Write C language programs to control dc motor, stepper motor and relay through ARM Cortex M4 microcontroller (POs: 1, 4, 5)
5. Write C language programs to interface keyboard, RTC and temperature sensor modules to ARM Cortex M4 microcontroller (POs: 1, 4, 5)

TECHNICAL SEMINAR – II

Course Code: MVE25 **Credits: 0:0:2**

Prerequisites: Nil **Contact Hours: 56**

LIST OF ACTIVITIES

1. Detailed discussion of block diagrams
2. Setting up the Simulation environment
3. Simulation of Results
4. Reproduction of Simulation Results: Written
5. Presentation of Simulation Results: Oral
6. Proposing a Technical block diagram: Written
7. Proposing a Technical block diagram: Oral
8. **REVIEW – 1**
9. Design of Experiments
10. Design of Experiments
11. Presentation of Simulation Results: Written
12. Presentation of Simulation Results: Oral
13. Comprehensive report writing
14. **REVIEW – 2**

Course Outcomes:

1. Present initial simulation results, replicating existing findings (POs: 1, 2, 3, 4, 5)
2. Propose a technical block diagram with arguments for improved performance (POs: 1, 2, 3, 4, 5)
3. Present the tools required for performing experiments, and justify their appropriateness (POs: 1, 2, 3, 4, 5)
4. Discuss simulation results and optimized performance metrics (POs: 1, 2, 3, 4, 5)
5. Discuss the advantages and disadvantages of approach, along with possible future directions (POs: 1, 2, 3, 4, 5)

EVALUATION RUBRICS

Criteria	Max Marks	Achievement Levels				CO Mapping
		Inadequate (0 – 33%)	**Developing (34 – 66%)**	**Proficient (67 – 100%)**	**Marks Awarded**	
Reproduction of existing results	**10**	Partial reproduction of results or large variation from reported results, no proper presentation using tables etc.	Partial reproduction of results, but no proper presentation and no analysis.	Complete reproduction of results, with appropriate tables/figures and analysis of results obtained.		**CO1**
Proposed Approach	**10**	No proper justification for methods used, or no new methods proposed.	New approach proposed, but without any justification.	New approach proposed, along with technical arguments that support the hypothesis.		**CO2**
Tool usage	**10**	Tool usage is not appropriate, is incorrect, or is incomplete.	Tools are used appropriately, but without knowledge of advanced options.	Tools are used appropriately, with complete knowledge of all available settings options suitable for analysis.		**CO3**
Results	**10**	Results are not indicative of proposed model, or are incomplete.	Results are complete, but are not better than existing solutions. Proper formats are used for presentation.	Results are presented using appropriate formats, and are better than existing solutions for the problem identified.		**CO4**
Discussion & Conclusions	**10**	No discussion of experiments and the results obtained.	Summary of experiments and results obtained thereby.	Summary of experiments and results obtained thereby, along with conclusions and future directions.		**CO5**
				TOTAL MARKS AWARDED		

LOW POWER VLSI DESIGN

Course Code: MVE31 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: V Anandi

UNIT – I

Power Dissipation in CMOS: Introduction, Need for low power VLSI chips, sources of power consumption, introduction to CMOS inverter power dissipation, low power VLSI design limits.

UNIT – II

Power Optimization: Logical Level Power Optimization: gate reorganization, local restructuring, signal gating, logic encoding, state machine encoding, pre-computation logic. Circuit Level Power Optimization: transistor and gate sizing, equivalent pin ordering, network restructuring and re-organization, special latches and flip-flops.

UNIT – III

Low Power Memory Design: Sources of power dissipation in DRAM & SRAM, low power techniques for SRAM, low power DRAM circuits Special techniques: power reduction and clock networks, low power bus, delay balancing.

UNIT – IV

Power Estimation: Simulation power analysis: SPICE circuit simulation, Gate level Simulation, Architectural level analysis, Data correlation analysis in DSP systems, Monte-Carlo simulation. Probabilistic power analysis: random signals, probabilistic techniques for signal activity estimation, propagation of static probability in logic circuits, gate level power analysis using transition density.

UNIT – V

Synthesis and Software Design for Low Power: Synthesis for low power: behavioral level transforms, algorithm level transforms for low power, architecture driven voltage scaling, power optimization using operation reduction, operation substitution. Software design for low power: gate level, architecture level, bus switching activity.

Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization.

References:

1. Gary Yeap, “Practical Low Power Digital VLSI Design”, Kluwer Academic Publishers, 2002.

2. K. Roy, S. C. Prasad, “Low Power CMOS VLSI Circuit Design”, Wiley, 2000, Indian Edition 2008.
3. Jan M. Rabaey, Massoud Pedram, “Low Power Design Methodologies”, KAP, 1996.
4. A. P. Chandrakasan, R. W. Broadersen, “Low Power Digital CMOS Design”, Kluwer, 1995

Course Outcomes:

1. Recall fundamental low power design concepts to classify power dissipation mechanisms in CMOS ICs (PO: 4)
2. Classify various power optimization techniques at circuit and logic level (PO: 4)
3. Design special circuits like clock generator, memories with special reference to speed and power consumption (POs: 1, 3, 4)
4. Analyze various power measurement and estimation techniques at different levels of abstraction and hence design power aware circuits (POs: 1, 4)
5. Analyze different architectural level low power transforms and logic synthesis techniques for DSP filters (POs: 1, 3, 4)

INTERNSHIP/INDUSTRIAL TRAINING

Course Code: MVE32 **Credits: 0:0:4**

Prerequisites: Nil

The evaluation of students will be based on an intermediate presentation, along with responses to a questionnaire testing for outcomes attained at the end of the internship. The rubrics for evaluation of the presentation and the questionnaire for the report will be distributed at the beginning of the internship.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels				CO Mapping
		Inadequate (0% – 33 %)	Developing (34% – 66%)	Proficient (67% – 100%)	Marks Awarded	
Complex Technical Blocks	**10**	No working knowledge of the domain.	Working knowledge of the domain, with some knowledge of internal details.	Detailed understanding of the system, along with underlying mechanisms.		**CO1**
Error Debugging	**10**	No ability to diagnose or correct errors, or improve performance.	An ability to diagnose errors, but not correct them, no intuition on improving performance.	Diagnose and correct erroneous system operation, and propose methods to improve system performance.		**CO2**
Professional and Ethical Behavior	**10**	No knowledge of the requirement of professional and ethical behavior.	Understands the requirement for professional and ethical behavior.	Can predict the effects of non-professional an un-ethical behavior in the workplace.		**CO3**
Engineering and Finance	**10**	Cannot make the connection between engineering decisions and their economic impact.	Predict the cost of engineering decisions.	Creates designs keeping their economic impact in mind.		**CO4**
Lifelong Learning	**10**	No understanding of the requirements for lifelong learning in the engineering profession.	Can present examples of the impact of lifelong learning in the engineering industry.	Can present examples of the impact of lifelong learning, along with predicting future areas of impact of life-long learning.		**CO5**
				TOTAL MARKS AWARDED		

Course Outcomes:

1. Analyze the working of complex technical systems/blocks (POs: 1, 3, 4)
2. Correct errors during functioning and improve the performance of complex technical systems/blocks (POs: 1, 3, 4)
3. Understand the importance of professional and ethical behavior in the engineering workplace (POs: 1, 3, 4)
4. Predict the effect of engineering decisions on financial matters (POs: 1, 3, 4)
5. Appreciate the requirements for constant technology updation (POs: 1, 3, 4)

PROJECT WORK – I

Course Code: MVE33 **Credits: 0:0:6**
Prerequisites: Nil

The students will be evaluated based on two oral presentations during the semester. In the presentations they will have to discuss the results of their literature survey and initial implementations of the design.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels Phase – I, Review – I				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Introduction	**5**	Introduction is not clear, or is not technically accurate.	Introduction is accurate, but no in-depth analysis of the domain.	Clear introduction to the domain, along with design decisions and their impacts.		**CO1**
Literature survey	**10**	Few sources of low quality, with no proper discussion of results.	Appropriate discussion of existing results, but quality of sources is low.	Comprehensive list of results presented from recent quality sources.		**CO2**
Methods comparison	**10**	Methods not explained and compared in terms of internal implementation details.	Advantages and disadvantages discussed, but not with reference to actual methods.	Detailed description of existing methods, along with their advantages and disadvantages.		**CO3**
TOTAL MARKS AWARDED						

Criteria	Max. Marks	Achievement Levels Phase – I, Review – II				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Methods discussion	**5**	No implementation level discussion of methods used in literature.	Brief discussion of tools used and results obtained therein.	Detailed discussion of tools used and their impact on the quality of results obtained in literature sources.		**CO3**
Initial Results	**10**	Initial results are not complete, or do not match that of existing literature.	Proper tools used to generate results, but are not same as existing literature.	Suitable tools used with appropriate conditions to generate initial results, and a discussion of the latter.		**CO4**
Technical Block Diagram	**10**	Technical block diagram proposing improvements is not technically justified.	Block diagram proposing improvements is technically justified.	Multiple block diagrams for optimization are presented, with a detailed analysis of the advantages and disadvantages of each approach.		**CO5**
TOTAL MARKS AWARDED						

Course Outcomes:

1. Introduce the technical area chosen and demonstrate that the focus of the study is on a significant problem worth investigation (POs: 1, 3, 4, 5)
2. Discuss existing/standard solution strategies for the problem identified and its deficiency in the current scenario (POs: 1, 2, 3, 4, 5)
3. Compare and contrast various research outcomes as part of a literature survey of quality published academic work (POs: 1, 3, 4, 5)
4. Replicate existing results by choosing appropriate tools/methods (POs: 1, 3, 4, 5)
5. Present a technical block diagram and justify its improved performance, with respect to existing methods, through technical arguments (POs: 1, 2, 3, 4, 5)

PROJECT WORK – II

Subject code: MVE41 **Credits: 0:0:22**
Prerequisites: Nil

The students will be evaluated based on two oral presentations, in which they will present their proposed solutions to the problem identified, and discuss the implementation details and results obtained.

EVALUATION RUBRICS

Criteria	Max. Marks	Achievement Levels Phase – II, Review – I				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Methods discussion	**10**	A discussion of methods for optimization is not based on technical arguments.	One or more block diagrams presented for optimization, but not justified with technical arguments.	One or more block diagrams presented for optimization, along with along with accurate technical arguments for justification.		**CO1**
Initial Results	**10**	Results are not matching expectations, or are not complete.	Complete results generated, but not an improvement on existing metrics.	Complete results generated with an improvement over existing approaches due to proposed block diagram.		**CO2**
Analysis	**5**	No discussion about qualitative nature of results.	Results are discussed along with justification for the outcomes.	Results are discussed with arguments for the qualitative nature, and scope for improvement.		**CO3**
TOTAL MARKS AWARDED						

Criteria	Max. Marks	Achievement Levels Phase – II, Review – II				CO Mapping
		Inadequate (0% – 33 %)	**Developing (34% – 66%)**	**Proficient (67% – 100%)**	**Marks Awarded**	
Design of Experiments	**10**	Few experiments conducted, with no relation to problem domain.	Significant experiments conducted, but with no structure and relation to problem domain.	Significant experiments conducted, with all relevant parameters being tested in an orderly manner, and with relevance to hypothesis.		**CO3**
Experimental Results	**10**	Few results, not covering all cases, and not optimizing performance.	Performance is moderately optimized with respect to existing approaches, but not to the level predicted by block diagram.	Significant improvement in results, matching predictions in technical block diagram.		**CO4**
Discussion	**5**	No qualitative or quantitative discussion of the method, and its key characteristics.	Method is discussed, but without arguments justifying the advantages and disadvantages of the approach.	Method is summarized in detail, along with technical arguments justifying the advantages and disadvantages of the proposed method.		**CO5**
TOTAL MARKS AWARDED						

Course Outcomes:

1. Present different methods for improving existing performance metrics with respect to existing literature, along with justified technical arguments (POs: 1, 2, 3, 4, 5)
2. Implement solutions proposed using appropriate software tools (POs: 1, 3, 4, 5)
3. Compare implemented solutions and choose the best possible option based on factors such as societal impact, cost, speed, and practicality (POs: 1, 3, 4, 5)
4. Perform extensive experimentation to prove hypothesis (POs: 1, 3, 4, 5)
5. Discuss the proposed methods pros and cons, and its applicability in different situations, along with scope for improvement (POs: 1, 2, 3, 4, 5)

ELECTIVES

ADVANCED EMBEDDED SYSTEMS

Course Code: MVEE01 **Credits: 4:0:0**

Prerequisites: Embedded Systems **Contact Hours: 56**

Course Coordinator: Suma K V

UNIT – I

Typical Embedded System: Core of the Embedded System, Memory, Sensors and Actuators, Embedded Firmware, Other System Components. Characteristics and Quality Attributes of Embedded Systems

UNIT – II

Embedded system design and development: System design and development, life-cycle models- the waterfall model, the V cycle model, the spiral model and rapid prototyping incremental, problem solving – five steps to design, the design process, identifying the requirements, formulating the requirements specifications, the system design specification, system specifications vs system requirements.

Hardware Software Co-Design and Program Modeling: Fundamental Issues in Hardware Software Co-Design, Computational Models in Embedded Design

UNIT – III

Embedded Hardware Design and Development: EDA Tools, How to Use EDA Tool, Schematic Design – Place wire, Bus , port , junction, creating part numbers, Design Rules check, Bill of materials, Netlist creation , PCB Layout Design – Building blocks, Component placement, PCB track routing.

Embedded Firmware Design and Development: Embedded Firmware Design Approaches, Embedded Firmware Development Languages

UNIT – IV

Software modeling: Introduction to UML,UML DIAGRAMS, Use cases, class diagrams, dynamic modeling with UML, Interaction diagrams, Sequence diagrams, Fork and Join, Branch and merge, Activity diagram, State chart diagrams, dynamic modeling with structural design methods.

UNIT – V

Real Time Operating Systems (RTOS) based Embedded System Design: Operating System basics, Types of OS, Tasks, Process and Threads, Multiprocessing and Multitasking, Threads, Processes and Scheduling: Putting them altogether, Task Communication, Device Drivers, How to choose an RTOS

References:

1. Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education Private Limited, 2009.
2. James K Peckol, "Embedded Systems – A Contemporary Design Tool", John Wiley, 2008.

Course Outcomes:

1. Identify the basic building blocks, characteristics and quality attributes of embedded systems (POs: 1, 4)
2. Analyze the complete life cycle of embedded system design and development (POs: 3, 4)
3. Design a printed circuit board for a given circuit by using the PCB design IDE (POs: 1, 3, 4)
4. Interpret the various computational models of software in embedded system design (POs: 1, 4)
5. Select the RTOS for real time embedded system design (POs: 1, 3, 4)

DIGITAL SYSTEM DESIGN USING HDL

Course Code: MVEE02 **Credits: 4:0:0**

Prerequisites: Digital Electronics **Contact Hours: 56**

Course Coordinator: Gangadharaiah S L

UNIT – I

Introduction and Methodology: Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology. **Number Basics**: Unsigned and Signed Integers, Fixed and Floating-point Numbers.

UNIT – II

Sequential Basics: Storage elements, Counters, Sequential Data paths and Control, Clocked Synchronous Timing Methodology.

UNIT – III

Memories and Implementation Fabrics: Concepts, Memory Types, Error Detection and Correction.

Implementation Fabrics: ICs, PLDs, Packaging and circuit Boards, Interconnection and signal Integrity.

UNIT – IV

System Verilog Simulation and Synthesis: System Verilog extension to Verilog, RTL and gate level modeling, RTL Synthesis, Subset of System Verilog, System Verilog simulation, Digital Synthesis, Modules, Procedural blocks.

UNIT – V

RTL Modeling Fundamentals: System Verilog Language rules. Module, Module instances, Hierarchy, Four state data Values, Datatypes, Variable Types, Net Types, Operators, Continuous Signal Assignments, Procedural Signal Assignments, Modeling Combinational logic and Sequential Logic.

References:

1. Peter J. Ashenden, "Digital Design: An Embedded Systems Approach using Verilog", Elsevier, 2010.
2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, 2nd Edition 2010.

3. Stuart Sutherland, "RTL Modeling with System Verilog for Simulation and Synthesis: using System Verilog for ASIC and FPGA Design", Create Space Independent Publishing Platform, 1st Edition, 2017.
4. Chris Spear, Greogory J Tumbush, "System Verilog for Verification – A Guide to Learning Test Bench Language Features", Springer, 2012.

Course Outcomes:

1. Apply the concepts of Verilog modeling to design and verify the operations of complex digital logic circuits (POs:1, 3, 4)
2. Design, model and test pipelined storage elements, sequential data path controllers based on signed, unsigned fixed point and floating point number systems with Verilog (POs:1, 3, 4)
3. Apply the concept of Verilog modeling to multi-port memories and FIFO datapaths and FSMs with respect to integrated circuits (POs: 1, 3, 4)
4. Understand the basics of System Verilog to simulate and synthesize digital systems (POs: 1, 3, 4)
5. Design and model the combinational and sequential circuits using System Verilog (POs: 1, 3, 4)

DIGITAL VLSI TESTING

Course Code: MVEE03 **Credits: 4:0:0**

Prerequisites: Digital System Design using HDL **Contact hours: 56**

Course Coordinator: Raghuram S

UNIT – I

Introduction: Role of testing, Testing during the VLSI life cycle, Challenges in VLSI testing, test economics, Yield, Fault coverage, Historical review of VLSI test technology.

Fault Modeling: Various fault models, Single Stuck-at fault – fault equivalence, fault collapsing

UNIT – II

Logic and Fault Simulation: Simulation Models, Algorithms for true value simulation, Algorithms for fault simulation, Statistical methods for fault simulation.

Testability Measures: Controllability and Observability, SCOAP Testability analysis, Simulation based testability analysis, RTL testability analysis.

UNIT – III

Combinational Circuit Test Generation: ATPG Algebras, Combinational ATPG Algorithms – Naïve example, D-Algorithm, PODEM, FAN

Sequential Circuit Test Generation: Time frame expansion method, Simulation-based sequential ATPG.

UNIT – IV

DFT and Scan Design: Ad-Hoc DFT, Scan based design.

Logic BIST: Test pattern generation, output response analyzer, BIST architectures, Memory BIST, Fault coverage enhancement

UNIT – V

Boundary Scan: Introduction and motivation, TAP controller and port, SOC test problems

Testing in the Nanometer range: Delay testing, Physical failures and soft errors, High-speed I/O testing.

References:

1. Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, "VLSI Test Principles and Architectures: Design for Testability", Morgan Kaufmann Publishers, 2006.
2. Michael L. Bushnell, Vishwani D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits", Kluwer Academic Publishers, 2002.
3. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems Testing and Testable Design", Wiley – IEEE Press, 1993.

Course Outcomes:

1. Create and manipulate fault models of VLSI circuits (POs: 1, 3, 4)
2. Perform fault simulations, and predict testability measures of digital circuits (POs: 1, 3, 4)
3. Generate optimized test patterns for combinational and sequential logic circuits (POs: 1, 3, 4)
4. Design scan chains and BIST modules for digital designs (POs: 1, 3, 4)
5. Employ boundary scan elements in design (POs: 1, 3, 4)

ADVANCED MICROCONTROLLERS

Course Code: MVEE04 **Credits: 4:0:0**

Prerequisites: Microcontrollers **Contact Hours: 56**

Course Coordinator: Suma K V

UNIT – I

Introduction to ARM Cortex M Processors: What are ARM Cortex M Processors, advantages of the Cortex M Processors, applications of the ARM Cortex M processors ,Technical overview, general information, Architecture – introduction, programmer's model, behavior of the application program status word, memory system, exceptions and interrupts, system control block, Debug.

UNIT – II

Instruction set of ARM Cortex M4: moving data within the processor, memory access, arithmetic operations, logic operations, shift and rotate instructions, data conversion operations, bit field processing, compare and test, program flow control, saturation operations, exception-related instructions, sleep mode-related instructions, memory barrier instructions.

UNIT – III

Low power and system control features of ARM Cortex M4: Low power designs, low power features – sleep modes, system control register, entering sleep mode, wake-up conditions, sleep-on-exit feature, SEVONPEND, sleep extension/wake-up delay, WIC, event communication interface, low power features using WFI &WFE instructions in programming.

Cortex M4 floating point unit: overview, floating point register overview, CPACR register, floating point register bank, FPSCR, FPCCR, FPCAR, FPDSCR, media and floating point feature registers.

UNIT – IV

Fault exceptions & fault handling of ARM Cortex M4: causes of faults, enabling fault handlers, fault status registers and fault address registers, analyzing faults.

UNIT – V

The Embedded System Development Environment: The Integrated Development Environment (IDE), Types of Files Generated on Cross-compilation, Disassembler/Decompiler, Simulators, Emulators and Debugging.

References:

1. Joseph Yiu, "The Definitive Guide to the ARM Cortex-M4", Newnes, (Elsevier), 3rd Edition, 2014.
2. Shibu. K. V., "Introduction to Embedded Systems", Tata McGraw Hill Education Private Ltd., 2nd Edition, 2009.
3. David A Patterson, John L Hennessy, "Computer Organization and Design – ARM Edition", Morgan Kauffman Publishers Elsevier, 4th Edition, 2010.

Course Outcomes:

1. Familiarize with the technical overview and architecture of ARM Cortex M4 (PO: 3)
2. Apply the technical knowledge of ARM Cortex M4 to build programs (POs: 1, 3, 4)
3. Illustrate the importance of low power mode and floating point features of ARM Cortex M4 (POs:1, 3, 4)
4. Identify the causes of failures in ARM Cortex M4 using fault exception mechanism (POs: 1, 4)
5. Analyze the working of debugger tools for embedded system design and development (POs: 1, 4)

ADVANCED DIGITAL LOGIC VERIFICATION

Course Code: MVEE05 **Credits: 4:0:0**

Prerequisites: Digital System Design using HDL **Contact Hours: 56**

Course Coordinator: Gangadharaiah S L

UNIT – I

Verification Concepts: Concepts of Verification, Importance of verification, Stimulus vs Verification, Test bench generation, Functional verification approaches, Typical verification flow, Stimulus generation, Direct testing ,Coverage: Code coverage and Functional coverage, Coverage plan.

UNIT – II

System Verilog – Language Constructs: System Verilog Constructs- Data types: Two state data, Strings, Arrays: Queues, Dynamic and Associative Arrays, Structs, Enumerated types. Program blocks, modules, interfaces, Clocking ports, Mod ports.

UNIT – III

System Verilog – Classes and Randomization: SV classes, Language evolution, Classes and Objects, Class Variables and Methods, Class Instantiation, Inheritance and Encapsulation, Polymorphism. Randomization: Directed vs Random Testing, Randomization: Constraint driven Randomization.

UNIT – IV

System Verilog – Assertions and Coverage: Assertions: Introduction to assertion based verification, Immediate and concurrent assertions, Coverage driven assertion: Motivation, types of coverage, Cover group, Cover point, Cross coverage, Concepts of binning and event sampling.

UNIT – V

Building Test bench: Layered test bench architecture, Introduction to Universal verification methodology, Overview of UVM, Base classes and simulation phases in UVM and UVM macros, Unified messaging in UVM, UVM environment structure, Connecting DUT-Virtual Interface.

References:

1. System Verilog LRM
2. Chris Spear, Greogory J Tumbush, “System Verilog for Verification – A guide to learning test bench language features”, Springer, 2012.

3. Sasan Iman, "Step by Step Functional Verification with System Verilog and OVM", Hansen Brown Publishing, 2008.
4. Stuart Sutherland, Simon Davidmann, Peter Flake, "System Verilog for Design – A guide to using System Verilog for hardware design and modeling", Springer Publications, 2nd Edition, 2006.
5. Janick Bergeron, "Writing Test Benches using System Verilog", Springer International Edition, 2009.
6. www.asic-world.com
7. www.testbench.in

Course Outcomes:

1. Discuss the principle and importance of verification (POs: 1, 3, 4)
2. Apply OOPs concepts in System Verilog to verify a digital system (POs: 1, 3, 4)
3. Develop basic verification environment using System Verilog (POs: 1, 3, 4)
4. Create random stimulus and track functional coverage using System Verilog (POs: 1, 3, 4)
5. Illustrate the concepts of layered test bench architecture and its components (POs: 1, 3, 4)

MEMS AND NANOELECTRONICS

Course Code: MVEE06 **Credits: 4:0:0**

Prerequisites: Semiconductors Theory **Contact Hours: 56**

Course Coordinator: Lakshmi S

UNIT – I

Introduction to MEMS and MEMS devices and systems: Feynman's vision, multi-disciplinary aspects, application areas. Scaling laws in miniaturization, scaling in geometry, electrostatics, electromagnetics.

Micro and Smart Devices and Systems – Principles: Transduction principles in MEMS Sensors: Actuators: different actuation mechanisms - silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, silicon micro-mirror arrays, piezo-electric based inkjet print head, electrostatic comb-driver.

UNIT – II

Micro manufacturing and Packaging: Lithography, thin-film deposition, etching (wet and dry), wafer-bonding, Silicon micromachining: surface, bulk, LIGA process, Wafer bonding process.

Integration and Packaging of MEMS devices: Integration of microelectronics and micro devices at wafer and chip levels, Microelectronic packaging: wire and ball bonding, flip chip, Microsystem packaging examples.

UNIT – III

Electrical and Electronics Aspects of MEMS: Electrostatics, Coupled electro mechanics, stability and Pull-in phenomenon, Practical signal conditioning circuits for microsystems, RF MEMS: Switches, varactors, tuned filters.

UNIT – IV

Introduction to Nanoelectronics: Particles and waves, Wave-particle duality, Wave mechanics, Schrödinger wave equation, Materials for nanoelectronics, Semiconductors, Crystal lattices: Bonding in crystals, Electron energy bands, Semiconductor heterostructures, Lattice-matched

and pseudomorphic heterostructures, Inorganic-organic heterostructures, Carbon nanomaterials: nanotubes and fullerenes.

Electron transport in nanostructures: Electrons in traditional low-dimensional structures, Electrons in quantum wells, Electrons in quantum wires, Electrons in quantum dots, Nanostructure devices, Resonant-tunneling diodes, Single-electron-transfer devices, Nano-electromechanical system devices, Quantum-dot cellular automata.

UNIT – V

Fabrication, Measurement and Applications: Fabrication and measurement techniques for nanostructures, Bulk crystal and heterostructure growth, Nanolithography, etching, other means for fabrication of nanostructures and nanodevices, Techniques for characterization of nanostructures, Spontaneous formation and ordering of nanostructures, Clusters and nanocrystals.

Applications: Injection Lasers: Quantum cascade lasers, Single photon sources, Biological tagging, Optical memories, Coulomb blockade devices, Photonic structures, QWIPs, NEMS, and MEMS.

References:

1. G. K. Ananthasuresh, K. J. Vinoy, S. Gopalakrishnan, K. N. Bhat, V. K. Aatre, "Micro and Smart Systems", Wiley India, 1st Edition, 2010.
2. T R Hsu, "MEMS and Microsystems Design and Manufacturing", Tata McGraw Hill, 2nd Edition, 2008.
3. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications", Cambridge University Press, 2011.
4. George W. Hanson, "Fundamentals of Nanoelectronics", Pearson Education India, 2009.

Course Outcomes:

1. Analyze scaling laws and operation of various practical MEMS systems (POs: 1, 3)
2. Describe various fabrication techniques and packaging methods for MEMS devices (PO: 3)
3. Identify the electronics and RF aspects of MEMS systems (POs: 3, 4)

4. Recognize the distinguishing aspect of nanoscale devices and systems (PO: 3)
5. Examine the basic science behind the design and fabrication of nano scale systems and their applications (PO: 3)

INTERNET OF THINGS

Course Code: MVEE07 **Credits: 4:0:0**

Prerequisites: Computer Networks **Contact Hours: 56**

Course Coordinator: Lakshmi S.

UNIT – I

Introduction & concepts: Definition and Characteristics of IoT, Things in IoT, IoT Protocols, IoT Functional Blocks, IoT Communication Models, IoT Communication APIs, IoT Enabling Technologies, IoT levels and deployment templates, IoT and M2M, SDN and NFV for IoT, IoT system management with NETCONFIG – YANG

UNIT – II

Developing Internet of Things: IoT Platform design methodology, Specifications: Requirements, Process, Domain, Information, Services, Level, Functional, Operational, Integration, Application Development

Python Language: Data Types and Data Structures, Control Flow, Functions, Modules, Packages, File Handling, Date and Time Operations, Classes, Python packages of interest for IoT

UNIT – III

IoT Physical Devices and End Points: Basic building blocks of an IoT Device, Raspberry Pi, Linux on Raspberry Pi, Raspberry Pi Interfaces: Serial, SPI, I2C

Programming Raspberry Pi with Python: Controlling LED, Interfacing Switch, Interfacing Light Sensor

UNIT – IV

Cloud and Data Analytics: Introduction to cloud storage models and communication APIs

Web Application Framework: Django, Web Services for IoT, SkyNet Messaging Platform, Data Analytics for IoT, Apache: Hadoop, Oozie, Storm, Real-Time Data Analysis, Tools for IoT

UNIT – V

IoT Case Studies: Home Automation: Smart Lighting, Home Intrusion Detection; Cities: Smart Parking Environment: Weather Monitoring System, Weather Reporting Bot, Air Pollution Monitoring, Forest Fire Detection; Agriculture – Smart Irrigation, IoT Printer, IOT in Automobiles: Intelligent Transportation and the Connected Vehicle, Vehicular Ad-hoc Networks (VANETs)

References:

1. Arshdeep Bahga, Vijay Madisetti, "Internet of Things: A Hands-on Approach", University Press, 2015.
2. Pethuru Raj, Anupama C Raman, "The Internet of things: Enabling Technologies, Platforms, and Use Cases Description", Taylor & Francis, CRC Press, 2017.
3. Daniel Minoli "Building the Internet of Things with IPV6, John Wiley & Sons, 2013.

Course Outcomes:

1. Describe the OSI Model for the IoT/M2M systems (POs: 1, 3)
2. Learn basics of design, integration and applications of IoT models (POs: 1, 3)
3. Acquire the knowledge of basic blocks of an IoT devices using Raspberry Pi (PO: 3)
4. Understand cloud storage models and web services for IoT (PO: 3)
5. Appraise with various case studies (POs: 1, 3, 4)

PHYSICS OF SEMICONDUCTOR DEVICES

Course Code: MVEE08 **Credits: 4:0:0**
Prerequisites: Solid State Devices and Circuits **Contact Hours: 56**
Course Coordinator: Raghuram S

UNIT – I

Energy Bands and Charge Carriers in Semiconductors: Bonding forces in solids, Energy Bands, Metals-Semiconductors-Insulators, Electrons and Holes, Effective mass, The Fermi Level, Electron and Hole concentrations in Equilibrium.

UNIT – II

Conductivity and Mobility: Effects of Temperature and Doping on Mobility, The Hall Effect, Carrier Lifetime, Direct and Indirect Recombination, Diffusion and Drift of Carriers, The Continuity Equation, Steady State Carrier Injection.

UNIT – III

PN Junctions: Contact potential, Fermi levels and Space charge, Junction Current, carrier injection, Time variation of stored charge, capacitance of pn junctions, Schottky Barriers, Rectifying and Ohmic contacts, Heterojunctions.

UNIT – IV

Bipolar Junction Transistors: Fundamental operation, amplification, Terminal currents, Cutoff and Saturation, Secondary Effects, Gummel Poon model, Capacitance and Charging time, Heterojunction bipolar transistors.

UNIT – V

MOS Capacitor and threshold voltage: MOSFET: Output and transfer characteristics, Short Channel I-V model, Control of Threshold Voltage, Substrate Bias Effect, Subthreshold characteristics, Equivalent circuit, Secondary effects, Advanced MOSFET Structures.

References:

1. Ben Streetman, Sanjay Bannerjee, "Solid State Electronic Devices", Prentice Hall India, 7th Edition, 2014.
2. Robert F Pierret, "Semiconductor Device Fundamentals", Addison Wesley, 2nd Edition, 1996.
3. Robert F Pierret, "Advanced Semiconductor Fundamentals", Prentice Hall, 2nd Edition, 1992.

Course Outcomes:

1. Estimate carrier concentration in semiconductors, given the type and doping level of impurities (POs: 3, 4)

2. Predict drift and diffusion carrier concentration in semiconductors (POs: 3, 4)
3. Compute the current through a pn junction, under forward and reverse biased conditions (POs: 3, 4)
4. Apply basic and advanced electronics concepts to derive models for current flow in a BJT transistor (POs: 3, 4)
5. Employ basic and advanced electronics concepts to predict qualitative and quantitative operating conditions of MOS transistors (POs: 3, 4)

SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS

Course Code: MVEE09 **Credits: 4:0:0**

Prerequisites: Digital Electronic Circuits **Contact Hours: 56**

Course Coordinator: S L Gangadhariah

UNIT – I

Introduction to Synthesis and optimization: Design of Microelectronics circuits, Computer aided Synthesis and Optimization.

Hardware Modeling: Abstract models, Compilation and Behavioral Optimization.

UNIT – II

Graph theory for CAD for VLSI: Graphs, Combinatorial Optimization, Graph Optimization problems and Algorithms, Boolean Algebra and Applications.

Architectural Synthesis and Optimization: Fundamental Architectural Synthesis problems, Area and Performance Estimation, Strategies for Architectural Optimization, Data path Synthesis, Control Path Synthesis.

UNIT – III

Two level Combinational Logic Optimization: Introduction, Logic Optimizations, operations on Two level Logic Covers, Algorithms for Logic Minimization, Symbolic Minimization and Encoding Problems, Minimization of Boolean relations

UNIT – IV

Multiple Level Combinational Logic Optimization: Introduction, Models and Transformations for Combinational Networks, Algebraic Model, Boolean Model.

Sequential Logic Optimization: Introduction, Sequential Logic Optimization using State based Models, Sequential Logic Optimization using Network Models, Implicit FSM Traversal Methods

UNIT- V

Scheduling Algorithms: Introduction, A Model for Scheduling problems, Scheduling with Resource Constraints, Scheduling without Resource Constraints, Scheduling Algorithms for Extended Sequencing Models, Scheduling Pipelined Circuits.

Resource Sharing and Binding: Sharing and Binding for Resource dominated circuits, Sharing and Binding for General Circuits, Concurrent Binding and Scheduling, Resource sharing and Binding for Non-scheduled Sequencing Graphs.

References:

1. Giovanni De Micheli, "Synthesis and Optimization of Digital Circuits", Tata McGraw-Hill, 2003.
2. Edwars M. D., "Automatic Logic synthesis Techniques for Digital Systems", Macmillan New Electronic Series, 1992.

Course Outcomes:

1. Appreciate the top down approach in design of digital circuits (POs: 1, 3, 4)
2. Apply the concepts of graph theory and its algorithm in optimization of Boolean equations (POs: 1, 3, 4)
3. Apply different two level logic optimization algorithms to combinational circuits (POs: 1, 3, 4)
4. Apply multilevel and sequential optimization algorithms to build digital circuits (POs: 1, 3, 4)
5. Implement different scheduling algorithms with and without resource binding for pipelined sequential circuits (POs:1, 3, 4)

ASIC DESIGN

Course Code: MVEE10 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: V. Anandi

UNIT – I

Introduction to ASICs: Full custom, Semi-custom and Programmable ASICs, ASIC Design flow, ASIC cell libraries.

CMOS Logic: Datapath Logic Cells**:** Data Path Elements, Adders: Carry skip, Carry bypass, Carry save, Carry select, Conditional sum, Multiplier (Booth encoding), Data path Operators, I/O cells.

UNIT – II

ASIC Library Design: Logical effort: Predicting Delay, Logical area and logical efficiency, Logical paths, Multi stage cells, Optimum delay and number of stages.

Programmable ASIC Logic Cells: MUX as Boolean function generators, Actel ACT: ACT 1, ACT 2 and ACT3 Logic Modules, Xilinx LCA: XC3000 CLB, Altera FLEX and MAX.

UNIT – III

Programmable ASIC I/O Cells: Xilinx and Altera I/O Block.

Low-level design entry: Schematic entry: Hierarchical design, Netlist screener.

ASIC Construction: Physical Design, CAD Tools.

Partitioning: Goals and objectives, Constructive Partitioning, Iterative Partitioning Improvement, KL and Look Ahead algorithms

UNIT – IV

Floor planning and placement: Goals and objectives, Floor planning tools, Channel definition, I/O and Power planning and Clock planning.

Placement: Goals and Objectives, Min-cut Placement algorithm, Iterative Placement Improvement, Physical Design Flow.

UNIT – V

Routing: Global Routing: Goals and objectives, Global Routing Methods, Back-annotation.

Detailed Routing: Goals and objectives, Measurement of Channel Density, Left-Edge and Area-Routing Algorithms. Special Routing, Circuit extraction and DRC

References:

1. M J S Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. Neil H. E. Weste, David Harris, Ayan Banerjee, "CMOS VLSI Design: A Circuits and Systems Perspective", 3rd Edition, Addison Wesley/Pearson Education, 2011.
3. Vikram Arkalgud Chandrasetty, "VLSI Design: A Practical Guide for FPGA and ASIC Implementations", Springer, 2011.
4. Rakesh Chadha, J. Bhasker, "An ASIC Low Power Primer: Analysis, Techniques and Specification", Springer Publications, 2015.

Course Outcomes:

1. Describe the concepts of ASIC design methodology, data path elements and FPGA architectures (PO: 4)
2. Design data path elements for ASIC cell libraries and compute optimum path delay (PO: 4)
3. Employ industry synthesis tools to achieve desired objectives (POs: 1, 2, 3, 5)
4. Analyze the design of FPGAs and ASICs suitable for specific tasks, perform design entry and explain the physical design flow. (POs: 1, 3, 4)
5. Create floor plan including partition and routing with the use of CAD algorithms (PO: 4)

SYSTEM ON CHIP DESIGN

Course Code: MVEE11 **Credits: 4:0:0**

Prerequisites: CMOS VLSI circuits **Contact Hours: 56**

Course Coordinator: A. R. Priyarenjini

UNIT – I

Motivation for SOC design: Review of Moore's law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance, Comparison of System-on-Board, System-on-Chip, and System-in-Package, Typical goals in SOC design – cost reduction, power reduction, design effort reduction, performance maximization.

UNIT – II

ASIC: Overview of ASIC types, Design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application specific Instruction Processor (ASIP) concepts.

UNIT – III

NISC: No instruction set computer**(**NISC) Control words methodology, NISC Application and Advantages, Architecture Description Languages(ADL) for design and verification of Application specific Instruction set Processors(ASIP), No-Instruction-set-computer(NISC)-design flow, modeling NISC architectures and systems, use of generic netlist representation.

UNIT – IV

Simulation: Different simulation modes, behavioral, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SOC related modeling of data path design and control logic, Minimization of interconnect impact, clock tree issues.

UNIT – V

Low power SOC design/Digital system: Design synergy, Low power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification.

References:

1. Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.

2. Rao R. Tummala, Madhavan Swaminathan, "Introduction to system on package SOP – Miniaturization of the Entire System", McGraw-Hill, 2008.
3. Hubert Kaselin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.
4. B. Al Hashimi, "System on chip – Next generation electronics", The IET, 2006.
5. Rochit Rajsuman, "System-on-a-chip: Design and Test", Advantest America R & D center, 2000.
6. Michael J Flynn and Wayne Luk, "Computer system design: System-on-chip", Wiley Publications, 2011.

Course Outcomes:

1. Compare SoB, SoC and SiP for electronic product in terms of size, cost, performance and reliability (POs: 3, 4)
2. Analyze different approaches for solving architectural issues of SOC design (POs: 1, 3, 4)
3. Discuss NISC and use of ADL (POs: 1, 3, 4)
4. Recognize different simulation modes and modeling of reconfigurable systems. (POs: 1, 3, 4)
5. Appraise low power SOC design (POs: 1, 3, 4)

PHYSICAL VLSI DESIGN

Course Code: MVEE12 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: Raghuram S

UNIT – I

Netlist Partition Algorithms: Introduction to Electronic Design Automation, Algorithms and Complexity, Graph Theory Terminology, Introduction to Netlists and System Partitioning,

Partitioning Algorithms: Kernighan-Lin algorithm

UNIT – II

Chip Planning: Introduction, Optimization goals in Floor planning, Floor plan representations

Floor Planning Algorithms: Floor plan sizing, cluster growth, simulated annealing, Pin assignment

Power and Ground Routing: design of power-ground distribution network, mesh routing. Integrated floor planning algorithms

UNIT – III

Global Placement and Routing: Introduction and objectives of placement, Global placement algorithms: min-cut placement, analytic placement, simulated annealing, ,Modern placement algorithms Routing terminology and goals

Single-Net Routing: Rectilinear routing, Dijsktra's algorithm, A*, Full net routing and Rip-up and Re-route. Global routing in a connectivity graph, Modern global routing, over the cell routing algorithms

UNIT – IV

Detailed and Specialized Routing: Building the Horizontal and Vertical Constraint Graphs, Leftedge algorithm, dog-legging, Switchbox routing, Introduction to area routing, Non-Manhattan routing, Routing in clock networks, clock-tree synthesis.

UNIT – V

Timing Closure: Introduction, Static Timing Analysis, Zero-slack algorithm, Timing driven placement, Timing driven routing, Physical synthesis, Performance Driven Design Flow

References:

1. Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu, "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer, 1st Edition, 2011
2. Sadiq M Sait and Habib Youssef, "VLSI Physical Design Automation", World Scientific Publishing, 1st Edition, 1995.
3. Navid A Sherwani, "Algorithms for VLSI Physical Design Automation", Springer, 3rd Edition, 2005.

Course Outcomes:

1. Apply basic partitioning algorithms to netlists (POs: 3, 4)
2. Compute the area using different floor planning algorithms (POs: 3, 4)
3. Predict the cost on the resultant wiring due to different place and route algorithms (POs: 3, 4)
4. Apply routing algorithms as applied to interconnect and clock networks (POs: 3, 4)
5. Choose appropriate interconnections in the presence of timing constraints (POs: 3, 4)

ADVANCED COMPUTER ARCHITECTURE

Course Code: MVEE13 **Credits: 4:0:0**

Prerequisites: Computer Organization **Contact Hours: 56**

Course Coordinator: V. Anandi

UNIT – I

Parallel Computer Models: The state of computing, Classification of parallel computers, Multiprocessors and multicomputer, Multivectors and SIMD computers Grain Size and latency

Program and Network Properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling.

UNIT – II

Program flow mechanisms: Control flow versus data flow, Comparisons of flow mechanisms, Performance Metrics and Measures Data flow Architecture, Demand driven mechanisms.

Principles of Scalable Performance: Parallel Processing Applications, Speedup Performance Laws, Scalability Analysis and Approaches.

UNIT – III

Speedup Performance Laws: Amdhal's law, Gustafson's law, Memory bounded speedup model, Scalability Analysis and Approaches.

Advanced Processors: Advanced processor technology, Instruction-set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors VLIW Architectures.

UNIT – IV

Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, branch prediction, Arithmetic Pipeline Design.

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, Multilevel cache hierarchies, main memory organizations, design of memory hierarchies.

UNIT – V

Multiprocessor Architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, scalable cache coherence, design challenges of directory protocols, memory based directory protocols, cache based directory

protocols. Cache coherence protocols (MSI, MESI, MOESI), overview of directory based approaches

References:

1. Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability", Tata McGraw Hill, 1st Edition, 2003.
2. Kai Hwang, Zu, "Scalable Parallel Computers Architecture" Tata McGraw Hill, 2003.
3. M. J. Flynn, "Computer Architecture, Pipelined and Parallel Processor Design", Narosa Publishing, 2002.
4. D. A. Patterson, J. L. Hennessy, "Computer Architecture: A Quantitative Approach", Morgan Kauffmann, 2012.

Course Outcomes:

1. Illustrate understanding of contemporary computer architecture issues and techniques (POs:1, 2)
2. Discuss the role of parallelism in current and future architectures (POs: 3)
3. Analyse the behavior of a processor pipeline as the processor executes various sequences of instructions (POs: 3, 4)
4. Apply concept and principle of cache memory and virtual memory to high performance computer architecture (POs: 1, 3, 5)
5. Compare different multi-processor architectures and cache coherence protocols (PO: 3)

VLSI SIGNAL PROCESSING

Course Code: MVEE14 **Credits: 4:0:0**

Prerequisites: Digital Signal Processing **Contact Hours: 56**

Course Coordinator: Gangadharaiah S L

UNIT – I

Introduction to DSP Systems: Typical DSP Algorithms, DSP Application Demands and Scaled CMOS Technologies, Representations of DSP Algorithms

Iteration Bounds: Data flow graph Representations, loop bound and Iteration bound, Algorithms for computing iteration bound, Iteration bound of multirate data flow graphs.

UNIT – II

Pipelining and Parallel Processing: Pipelining of FIR Digital Filters, parallel processing, Pipelining and parallel processing for low power

Retiming: Definition and Properties, Solving Systems of Inequalities, Retiming Techniques

UNIT – III

Unfolding: An Algorithm for Unfolding, Properties of Unfolding, Critical path, Unfolding and Retiming, Application of Unfolding.

Folding: Folding Transformation, Register minimization Techniques, Register minimization in Folded Architectures

Fast Convolution: Cook-Toom Algorithm, Winograd Algorithm, Iterated convolution, cyclic convolution Design of fast convolution Algorithm by Inspection.

UNIT – IV

Algorithmic strength reduction techniques: 2-parallel FIR filter, 2-parallel fast FIR filter, DCT architecture, rank-order filters, Odd-Even merge-sort architecture, parallel rank-order filters. Look-Ahead pipelining in first-order IIR filters, Look Ahead pipelining with power of 2 decomposition, Clustered look-ahead pipelining, Parallel Processing for IIR Filters, Combined pipelining and parallel processing for IIR Filter, Low power IIR Filter Design Using Pipelining and parallel processing.

UNIT – V

Bit-level arithmetic architectures: Parallel multipliers with sign extension, parallel carry-ripple array multiplier, parallel carry-save array multiplier, Baugh –Wooley Multiplier, Parallel Multipliers with Modified Booth Recording, Design of Lyon's bit-serial multipliers using Horner's rule, bit-serial FIR filter, CSD representation, CSD multiplication using Horner's rule for precision improvement, Distributed Arithmetic

References:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems, Design and Implementation", Wiley, Interscience, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Gate Arrays", Springer, 2nd Edition, 2004.
3. Roger Woods, John McAllister, Gaye Lightbody, Ying Yi, "FPGA based Implementation of Signal Processing Systems", John Wiley, 2008.
4. S. Y. Kung, H. J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.
5. Jose E. France, Yannis Tsividis, "Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.
6. Lars Wanhammar, "DSP Integrated Circuits", Academic Press Series in Engineering, 1st Edition, 1999.

Course Outcomes:

1. Illustrate the use of various DSP algorithms and their representation using block diagrams, signal flow graphs and data-flow graphs (POs: 1, 3, 4)
2. Apply the concept of pipelining, retiming and parallel processing in design of high-speed low power applications (POs: 1, 3, 4)
3. Apply unfolding, folding and fast convolution in the design of VLSI architecture (POs: 1, 3, 4)
4. Employ the algorithmic strength reduction techniques to VLSI implementation of filters (POs: 1, 3, 4)
5. Apply bit level arithmetic architectures for VLSI implementation of various DSP applications (POs: 1, 3, 4)

MEMORY TECHNOLOGIES

Course Code: MVEE15 **Credits: 4:0:0**

Prerequisites: CMOS VLSI Circuits **Contact Hours: 56**

Course Coordinator: V. Anandi

UNIT – I

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

UNIT – II

DRAM: MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs. SRAM and DRAM Memory controllers

UNIT – III

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

UNIT – IV

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

UNIT – V

Memory Hybrids: Memory Hybrids – 2D & 3D, Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

References:

1. Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Publications, 2002.
2. Kiyoo Itoh, "VLSI memory chip design", Springer Series in Advanced Microelectronics,1st Edition, 2001.
3. Ashok K Sharma, "Semiconductor Memories: Technology, Testing and Reliability", PHI, 1997.

Course Outcomes:

1. Recall random access memory classification and understand their operation (POs:1, 4)
2. Analyse the operation of advanced architectures of Dynamic RAMs (POs:1, 4)
3. Differentiate between the behavior of various ROMs and flash memories (PO: 4)
4. Illustrate understanding of contemporary and advanced memory technologies (POs: 1, 4)
5. Apply concept of testing on memories and understand different memory packaging technologies (PO: 4)

COMMUNICATION BUSSES AND INTERFACES

Course Code: MVEE16 **Credits: 4:0:0**

Prerequisites: Analog Communication **Contact Hours: 56**

Course Coordinator: Deepali Koppad

UNIT – I

Serial Busses: Physical interface, Data and Control signals, features

UNIT – II

Serial Busses: Limitations and applications of RS232, RS485, I2C, SPI

UNIT – III

CAN: Architecture, Data transmission, Layers, Frame formats, applications

UNIT – IV

PCI: Revisions, Configuration space, Hardware protocols, applications

UNIT – V

UCB: Transfer types, enumeration, Descriptor types and contents, Device driver, Data Streaming Serial Communication Protocol - Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

References:

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2nd Edition, 2007.
2. Jan Axelson, "USB Complete", Penram Publications, 5th Edition, 2007.
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press, 2012.
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.

Course Outcomes:

1. Recall various communications protocols and interface busses (POs: 1, 4)
2. Illustrate understanding of contemporary serial busses and limitations (POs: 1, 4)
3. Discuss CAN architecture and different frame formats (POs:1, 3, 4)
4. Compare various hardware protocols and their applications (PO: 4)
5. Apply data transfer concepts and serial communication protocols on serial busses (POs: 1, 4)