CURRICULUM

for the Academic year 2018 – 2019

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

V & VI Semester B. E.

RAMAIAH INSTITUTE OF TECHNOLOGY
(Autonomous Institute, Affiliated to VTU)
BANGALORE – 54
About the Institute

Ramaiah Institute of Technology (RIT) (formerly known as M. S. Ramaiah Institute of Technology) is a self-financing institution established in Bangalore in the year 1962 by the industrialist and philanthropist, Late Dr. M S Ramaiah. The institute is accredited with A grade by NAAC in 2016 and all engineering departments offering bachelor degree programs have been accredited by NBA. RIT is one of the few institutes with faculty student ratio of 1:15 and achieves excellent academic results. The institute is a participant of the Technical Education Quality Improvement Program (TEQIP), an initiative of the Government of India. All the departments are full with competent faculty, with 100% of them being postgraduates or doctorates. Some of the distinguished features of RIT are: State of the art laboratories, individual computing facility to all faculty members. All research departments are active with sponsored projects and more than 130 scholars are pursuing PhD. The Centre for Advanced Training and Continuing Education (CATCE), and Entrepreneurship Development Cell (EDC) have been set up on campus. RIT has a strong Placement and Training department with a committed team, a fully equipped Sports department, large air-conditioned library with over 80,000 books with subscription to more than 300 International and National Journals. The Digital Library subscribes to several online e-journals like IEEE, JET etc. RIT is a member of DELNET, and AICTE INDEST Consortium. RIT has a modern auditorium, several hi-tech conference halls, all air-conditioned with video conferencing facilities. It has excellent hostel facilities for boys and girls. RIT Alumni have distinguished themselves by occupying high positions in India and abroad and are in touch with the institute through an active Alumni Association. RIT obtained Academic Autonomy for all its UG and PG programs in the year 2007. As per the National Institutional Ranking Framework, MHRD, Government of India, Ramaiah Institute of Technology has achieved 60th rank in 2018 among the top 100 engineering colleges across India.

About the Department

The Department of Electronics and Communication was started in 1975 and has grown over the years in terms of stature and infrastructure. The department has well equipped simulation and electronic laboratories and is recognized as a research center under VTU. The department currently offers a B. E. program with an intake of 120, and two M. Tech programs, one in Digital Electronics and Communication, and one in VLSI Design and Embedded Systems, with intakes of 30 and 18 respectively. The department has a Center of Excellence in Food Technologies sponsored by VGST, Government of Karnataka. The department is equipped with numerous UG and PG labs, along with R & D facilities. Past and current research sponsoring agencies include DST, VTU, VGST and AICTE with funding amount worth Rs. 1 crore. The department has modern research ambitions to develop innovative solutions and products and to pursue various research activities focused towards national development in various advanced fields such as Signal Processing, Embedded Systems, Cognitive Sensors and RF Technology, Software Development and Mobile Technology.
Vision of the Institute

To evolve into an autonomous institution of international standing for imparting quality technical education

Mission of the Institute

MSRIT shall deliver global quality technical education by nurturing a conducive learning environment for a better tomorrow through continuous improvement and customization

Quality Policy

We at M. S. Ramaiah Institute of Technology strive to deliver comprehensive, continually enhanced, global quality technical and management education through an established Quality Management System complemented by the synergistic interaction of the stakeholders concerned

Vision of the Department

To be, and be recognized as, an excellent Department in Electronics & Communication Engineering that provides a great learning experience and to be a part of an outstanding community with admirable environment.

Mission of the Department

To provide a student centered learning environment which emphasizes close faculty-student interaction and co-operative education.

To prepare graduates who excel in the engineering profession, qualified to pursue advanced degrees, and possess the technical knowledge, critical thinking skills, creativity, and ethical values.

To train the graduates for attaining leadership in developing and applying technology for the betterment of society and sustaining the world environment.
Program Educational Objectives (PEOs):

PEO1: To train to be employed as successful professionals in a core area of their choice

PEO2: To participate in lifelong learning/ higher education efforts to emerge as expert researchers and technologists

PEO3: To develop their skills in ethical, professional, and managerial domains

Program Outcomes (POs):

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10: **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one’s own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs):

PO1: **Circuit Design Concepts**: Apply basic and advanced electronics for implementing and evaluating various circuit configurations

PO2: **VLSI and Embedded Domain**: Demonstrate technical competency in the design and analysis of components in VLSI and Embedded domains

PO3: **Communication Theory and Practice**: Possess application level knowledge in theoretical and practical aspects required for the realization of complex communication systems
CURRICULUM COURSE CREDITS DISTRIBUTION

<table>
<thead>
<tr>
<th>Semester</th>
<th>Humanities &amp; Social Sciences (HSS)</th>
<th>Basic Sciences / Lab (BS)</th>
<th>Engineering Sciences/ Lab (ES)</th>
<th>Professional Courses - Core (Hard core, soft core, Lab) (PC-C)</th>
<th>Professional Courses - Electives (PC-E)</th>
<th>Other Electives (OE)</th>
<th>Project Work/Internship (PW/IN)</th>
<th>Extra &amp; Co-curricular activities (EAC)</th>
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## SCHEME OF TEACHING

### V SEMESTER

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**Total** | 17 | 2 | 3 | 3 | 25 | 37 |

### VI SEMESTER

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**Total** | 12 | 1 | 9 | 3 | 25 | 38 |
## List of Electives

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<td>Speech Processing</td>
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<td>Low Power VLSI design</td>
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<td>Object Oriented Programming with C++</td>
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<td>ECE06</td>
<td>Digital System Design using Verilog</td>
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<td>DSP Architecture &amp; Algorithms</td>
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<td>MEMS</td>
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<td>Artificial Neural Networks &amp; Fuzzy Logic</td>
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<td>Image Processing</td>
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<td>ECE11</td>
<td>Real Time Systems</td>
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<td>Advanced Digital Logic Design</td>
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<td>Advanced Digital Logic Verification</td>
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<td>Linear Algebra</td>
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<td>Machine Learning</td>
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<td>Advanced Embedded Systems</td>
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<td>Modeling and Simulation of Data Networks</td>
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<td>Cyber Security</td>
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<td>Distributed Systems</td>
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<td>Internet Engineering</td>
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<td>Multimedia Communication</td>
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<td>Ad-hoc Wireless Networks</td>
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<td>Cryptography and Network Security</td>
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<td>ECE30</td>
<td>Advanced Computer Architecture</td>
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</table>
ANALOG COMMUNICATION

Course Code: EC51
Prerequisites: Signals and Systems
Course Coordinator: Mrs. Lakshmi S

UNIT – I


UNIT – II


Vestigial Side-band Modulation: Frequency domain description, Generation of VSB modulated wave, time domain description, coherent demodulation, envelope detection of VSB wave along with carrier.

UNIT – III


UNIT – IV

Applications of AM and FM: AM radio (super heterodyne): Block diagram of transmitter and receiver, mixer, AGC, performance characteristics. FM radio: block diagram of transmitter and receiver.

Elements of Color TV: Frequency range and channel bandwidth, scanning and synchronization, composite video signal. Block diagram of transmitter and receiver.
UNIT – V

Noise Basics and Noise in Continuous Wave Modulation Systems: Introduction, shot noise, thermal noise, white noise, noise equivalent bandwidth, noise figure, equivalent noise temperature, cascade connection of two port networks, receiver model, noise in DSBSC receivers, noise in SSB receivers, noise in AM receivers, threshold effect, noise in FM receivers, FM threshold effect, pre-emphasis and de-emphasis in FM.

Textbooks:


References:


Course Outcomes:

1. Analyze the generation and demodulation of AM and DSBSC systems (POs – 1, 2, 3, 4, 12, PSOs – 1, 3)
2. Realize the generation and demodulation of SSB and VSB (POs – 1, 2, 3, 4, 12, PSOs – 1, 3)
3. Discuss the direct and indirect method of generation of FM and its detection (POs – 1, 2, 3, 4, 12, PSOs – 1, 3)
4. Apply AM and FM basics in radio and TV systems (POs – 2, 3, 12, PSOs – 1, 3)
5. Analyze the noise performance of receivers (POs – 1, 2, 12, PSOs – 1, 3)
CMOS VLSI DESIGN

Course Code: EC52  Credits: 3:0:0:1
Prerequisites: Digital Electronic Circuits  Contact Hours: 42
Course Coordinator: Mrs. A. R. Priyarenjini

UNIT – I

CMOS Logic and Layouts: Introduction and history, CMOS Logic Circuits: Logic Gates, Pass Transistor and Transmission gates


UNIT – II


UNIT – III


UNIT – IV

Combinational Circuit Design: Circuit Families: Static CMOS, Ratioed Circuits, CVSL, Dynamic Circuits, Pass Transistor Circuits.

UNIT – V

Data path Subsystems: Adders: Ripple carry, Carry Generate and Propagate, Propagate Generate Logic, Manchester Carry Chain, Carry Skip, Carry Select, Carry Look ahead, Tree Adders, Subtraction, Multiple-Input Addition.

Textbooks:


References:


Course Outcomes:

1. Create MOS schematics and corresponding layouts for simple digital logic functions. (PO – 2, 3, 4, 5, 9, 10, 11, PSO – 2)
2. Calculate various circuit parameters such as current and device capacitance for a MOS transistor. (PO – 2, 3, 4, 5, 9, 10, 11, PSO – 2)
3. Evaluate the delay due to a MOS logic circuit, and thereby design a circuit to satisfy certain design parameters. (PO – 2, 3, 4, 5, 9, 10, 11, PSO – 2)
4. Analyze the performance of various MOS circuit families. (PO – 2, 3, 4, 5, 9, 10, 11, PSO – 2)
5. Describe various connection configurations to realize digital adder designs and analyze their operating speed. (PO – 2, 3, 4, 5, 9, 10, 11, PSO – 2)
DIGITAL SIGNAL PROCESSING

Course Code: EC53  
Prerequisite: Signals and Systems  
Course Coordinator: Dr. K. Indira

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<th>UNIT – I</th>
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<tr>
<td><strong>Sampling and Reconstruction of Signals</strong>: Ideal sampling and reconstruction of continuous time signals, discrete time processing of continuous time signals.</td>
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<tr>
<td><strong>Frequency Domain analysis of LTI systems</strong>: Frequency domain characteristics of LTI systems, Frequency response of LTI systems, Frequency Domain Sampling and Reconstruction of discrete time signals.</td>
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<td><strong>FIR Filters</strong>: Design of FIR filters: Symmetric and anti-symmetric FIR filters, Design of linear-phase FIR filters using windows and frequency sampling methods, FIR differentiators.</td>
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<td><strong>Structures for FIR Systems</strong>: Direct-Form Structures, Cascade-Form Structures and Lattice Structures.</td>
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<td><strong>IIR filter structures</strong>: Direct form (I and II), Cascade, Parallel, and Transposed structures</td>
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<tr>
<td><strong>Architecture and Instruction set of TMS320C67x Processor</strong>: Architecture, Addressing modes, Instruction sets, Assembler directives, Memory considerations, Fixed and Floating point formats, implementation of FIR and IIR filters.</td>
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Textbooks:


References:


Course Outcomes:

1. Illustrate the importance of sampling and frequency domain analysis of LTI Systems. (POs – 1, 2. PSO – 3)
2. Apply DFT in linear filtering. (POs – 2, 3. PSO – 3)
3. Design and develop digital structures for FIR filters. (POs – 2, 3. PSO – 3)
4. Design and develop digital structures for IIR filters. (POs – 2, 3. PSO – 3)
5. Summarize the architecture and instruction sets of TMS32067x processor. (POs – 2, 3. PSO – 3)
TRANSMISSION LINES AND RADIATING SYSTEMS

Course Code: EC54
Prerequisite: Electromagnetics
Course Coordinator: Mrs. Sujatha B

UNIT – I

Transmission Line theory: Lumped element circuit model for a transmission line, wave propagation on a transmission line and general solutions of line, terminated lossless line, characteristic impedance, reflection coefficient, VSWR and impedance equation. Special cases of terminated lossless line, Smith chart: construction and applications, Conventional and graphical solution of line parameters.

UNIT – II


UNIT – III

Transmission lines and Fundamentals of radiator: Co-axial line, Strip line and Micro strip line, Principle of antenna, fields from oscillating dipole, antenna field zones, basic antenna parameters, patterns, beam area, Radiation intensity, beam efficiency, directivity and gain, antenna aperture, effective height and radio communication link (Friis formula).

UNIT – IV

Point source and Arrays: Point source, Types of Arrays (Broad side, End fire, Extended End fire), Arrays of two point sources, linear array of n-isotropic point sources of equal amplitude and spacing, Null direction for arrays n isotropic point source of equal amplitude and spacing, pattern multiplication.

UNIT – V

Thin linear antenna, Horn antenna and Parabolic reflectors: Introduction, short electric dipole, Fields of short electric dipole, radiation resistance of short electric dipole, thin linear antenna, field components of λ/2 (hertz) dipole antenna, radiation resistance of λ/2 antenna, Directivity of dipole antenna, Types of antenna – Yagi-Uda antenna, Horn antenna, parabolic reflectors.

Textbooks:

References:


Course Outcomes:

1. Analyze various transmission lines and find there parameters analytically and graphically. (POs – 1, 2, 3, 12, PSOs – 1, 2).
2. Apply Smith chart to design various impedance matching networks and also analyze line resonators. (POs – 1, 2, 3, 12, PSOs –1, 2).
3. Define the parameters of antenna. (POs – 1, 2, 3, 12, PSOs – 1, 3).
4. Design different types of arrays and study the concept of pattern multiplication. (POs – 1, 2, 3, 12, PSOs –1, 3).
5. Explore the field components and radiation resistance of various antennas. (POs – 1, 2, 3, 12, PSOs –1, 3).
MANAGEMENT, ENTREPRENEURSHIP AND IPR

Course Code: EC55  
Prerequisite: Nil  
Course Coordinator: Mr. V. Nuthan Prasad

Credits: 1:0:0:1  
Contact Hours: 14

UNIT – I

Management: Introduction, functions of management, Roles of manager, Levels of management, Development of management thought.

Planning: Planning process, Types of plans (meaning only), Steps in planning, Decision making.

Organizing and Staffing: Principles of organization, Types of organization, Importance of staffing.

UNIT – II

Directing and Controlling: Principles of directing, Leadership styles, Techniques and importance of coordination and steps in controlling.

Entrepreneur: Functions of an entrepreneur, Stages in entrepreneurial process.

UNIT – III

SSI: Role of SSI in Economic Development, Steps to start an SSI

Project Management: Project Identification, Project selection

Entrepreneurship Development and Government: KIADB, MSME, SIDBI

UNIT – IV

IPR: Basic Principles of IPR laws, history of IPR – GATT, WTO, WIPO and TRIPS, role of IPR in R&D and Knowledge era, concept of property, justification, Marx’s theory of property, different forms of IPR.

UNIT – V

Patent: Evolution of patent law in India, Justifications, subject matters of patent, Criteria for patentability, patentable and non-patentable inventions, pre-grant and post-grant oppositions, grant or refusal of patents.
**Patent application procedure and drafting:** Patent drafting, format, provisional and complete specifications, scopes of invention, claims, patent search and types of patent searches.

**Self-Study:** Modern management approaches, planning premises, Departmentation, committees, communication meaning and importance, methods of establishing control (in brief). Types of Entrepreneur, role of Entrepreneur in Indian economy and developing economies with reference to Self-employment development, impact of liberalization, privatization globalization on SSI, project report, KSFC, constitutional aspects of intellectual property, infringement of patents and design rights

**Textbooks:**
4. T. Ramakrishna, “Course Material for I Year P. G. Diploma in IPR”, NLSIU, Bangalore

**References:**

**Course Outcomes:**
1. Identify the importance of managerial discipline. (POs – 1, 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, PSO – 2)
2. Interpret the concepts of directing and controlling. (POs – 1, 2, 5, 7, 8, 9, 10, 11, 12, PSO – 2)
3. Demonstrate the functions of an entrepreneurship development and describe various institutional supports (POs – 1, 4, 5, 6, 7, 8, 9, 10, 11, 12, PSO – 3)
4. Describe the basic principles of different IPRs (POs – 2, 7, 9, 10, 11, 12, PSO – 3)
5. Recognize the characteristics and infringement of patents (POs – 5, 6, 8, 9, 10, 11, 12, PSO – 3)
ANALOG COMMUNICATION AND LIC LABORATORY

Course Code: ECL56                                      Credits: 0:0:1:0
Prerequisites: Analog Electronic Circuits Laboratory    Contact Sessions: 14
Course Coordinator: Mrs. Lakshmi S

LIST OF EXPERIMENTS

1. Differentiator and integrator using op-amps
2. Second order active low pass and high pass filter
3. Precision rectifier & 723 Regulator
4. Class-C amplifier
5. Generation and demodulation of AM
6. Schmitt Trigger
7. Generation of DSBSC using ring modulation
8. 555 Timer: Astable and Monostable Multivibrators
9. Generation and demodulation of FM
10. R-2R Ladder type Analog to Digital Converter and Flash ADC
11. Up conversion and down conversion using transistor mixer
12. Simulation of analog modulation techniques

Textbooks:


Course Outcomes:

1. Analyze basic op-amp circuits to perform differentiation and integration. (POs – 1, 2, 3, 4, 9, 10, PSOs – 1, 3)
2. Design, simulate and implement modulation and demodulation circuits for AM and FM (POs – 1, 2, 3, 4, 5, 9, 10, PSOs – 1, 3)
3. Test analog filters, precision rectifier and regulators for the given specifications (POs – 1, 2, 3, 4, 9, 10, PSOs – 1, 3)
4. Implement multivibrators using IC 555 timer for the given specifications (POs – 1, 2, 3, 4, 9, 10, PSOs – 1, 3)
5. Construct analog to digital converters. (POs – 1, 2, 3, 4, 9, 10. PSOs –1, 3)
LIST OF EXPERIMENTS

Simulation Experiments
1. Verification of Sampling Theorem
2. DFT and IDFT, Circular convolution and Linear convolution
3. Design and implementation of FIR Filters (LP, HP, BP, BS) by using window techniques
4. Design and implementation of analog IIR Filters (Butterworth and Chebyshev)
5. Design and implementation of digital IIR Filters (Bilinear transformation)

Hardware Experiments
6. Linear convolution and Circular convolution
7. Computation of N point DFT/IDFT
8. Response of a discrete time system
9. Design and implementation of digital FIR Filters
10. Design and implementation of digital IIR Filters
11. Filtering of noisy signal using FIR Filter
12. Generating signals of different frequencies and construction of AM wave

Textbooks:

Course Outcomes:
1. Apply sampling theorem on continuous time signal. (POs – 1, 2, 3, 5, 9, PSO – 3)
2. Apply DFT and IDFT in linear and circular convolutions. (POs –1, 2, 3, 5, 9, PSO – 3)
3. Analyze the frequency response of FIR and IIR filters. (POs – 2, 3, 5, 9, PSO – 3)
4. Demonstrate filtering of noisy signals. (POs – 2, 3, 4, 5, 9, PSO – 3)
5. Discuss generation of AM wave. (POs – 2, 3, 4, 5, 9, PSO – 3)
LIST OF EXPERIMENTS

All the experiments will make use of appropriate design tools.

1. Introduction to Design Entry and Simulation
2. Netlist generation, power, area, and timing report generation
3. NMOS and PMOS DC Analysis
4. Device Characterization
5. CMOS Inverter DC and Transient analysis
6. Propagation delay of various simple gates, and comparison with logical effort
7. Fanout-of-4 Inverter delay measurement in different technologies
8. Verification of method of Logical effort
9. Inverter Chain Sizing
10. Verification of Full adder implementations at the transistor level
11. Inverter Layout Design and Post layout simulation

Textbook:

Course Outcomes:
1. Employ the digital design tools for HDL design entry, simulation, and synthesis. (POs – 2, 3, 4, 5, 9, 10, PSO – 2)
2. Create and verify functionality of various gates at the transistor level. (POs – 2, 3, 4, 5, 9, 10, PSO – 2)
3. Measure circuit performance parameters by performing simulations of circuit configurations. (POs – 2, 3, 4, 5, 9, 10, PSO – 2)
4. Use tools to characterize processes by conducting suitable experiments. (POs – 2, 3, 4, 5, 9, 10, PSO – 2)
5. Create the layout for simple gates, and perform RC extraction and post layout simulation. (POs – 2, 3, 4, 5, 9, 10, PSOs – 2)
DIGITAL COMMUNICATION

Course Code: EC61  
Prerequisites: Analog Communication  
Course Coordinator: Mr. Sadashiva V Chakrasali

Credits: 3:1:0:0  
Contact Sessions: 56

UNIT – I

Signal Sampling: Basic signal processing operations in digital communication, Sampling Principles, Sampling Theorem, Quadrature sampling of band-pass signals, Practical aspects of sampling and signal recovery, PAM, TDM.

UNIT – II

Waveform Coding Techniques: PCM block diagram, Different quantization techniques, SNR in PCM Robust quantization, DPCM, DM, Adaptive DM.

Base-Band Shaping for Data Transmission: Line Codes and their power spectra.

UNIT – III

Inter symbol interference: Introduction, Nyquist criterion for distortion less base-band binary transmission, correlative coding, duo binary coding, Eye pattern.

Detection: Model of digital communication system, Gram – Schmidt orthogonalization, geometric interpretation of signals, Maximum likelihood estimation.

UNIT – IV


Digital Modulation and Demodulation Techniques: Coherent binary modulation techniques, BPSK, FSK, ASK, QPSK systems with signal space diagram, generation, demodulation and error probability concept, Comparison using Power Spectrum.

UNIT – V

Non coherent modulation techniques: FSK and BPSK, DPSK.
**Spread spectrum modulation:** Pseudo noise sequences, Notion of spread spectrum, direct sequence spread coherent BPSK, Signal space dimensionality and processing gain, Frequency Hop spread spectrum and applications of spread spectrum modulation.

**Textbooks:**


**References:**


**Course Outcomes:**

1. Design a system to convert the given analog signal into discrete signal. (POs – 1, 2, 3, 8, 11, PSO – 3)
2. Analyze PCM, DPCM, DM and ADM systems and Base Band shaping for data transmission. (POs – 1, 2, 3, 4, 8, 11, PSO – 3)
3. Describe effects of ISI and detect message signal in noisy environment. (POs – 1, 2, 3, 4, 8, 11, PSO – 3)
4. Compare performance of BPSK, ASK, and QPSK systems and their power spectra. (POs – 1, 2, 3, 8, 11, PSO – 3)
5. Describe spread spectrum technology and its applications. (POs – 1, 2, 3, 8, 11. PSO – 3)
MICROCONTROLLER

Course Code: EC62  
Credits: 3:0:0:1
Prerequisite: Microprocessors  
Contact Hours: 42
Course Coordinator: Mrs. Sara Mohan George

UNIT – I

The MSP430 Architecture: The outside view-pin out, the inside view, memory, CPU, Memory mapped input output Addressing Modes, Constant generator and emulated instructions, Instruction set, examples

UNIT – II

Functions and subroutines: Storage for local variables, passing parameters to a subroutine and returning a result, mixing C and assembly language, interrupts, interrupt service routines, interrupt service routines in C, non-maskable interrupts, issues associated with interrupts, Low power modes

Digital input, output and displays: Parallel ports, digital inputs, interrupts on digital inputs, multiplexed inputs: scanning a matrix keypad, Digital outputs: multiplexed displays.

UNIT – III

Timers: Watchdog timer, timer A: Timer block, capture/compare channels, interrupts from timer A, Measurement in the capture mode: Measurement of time; Press and release of button, Output in the continuous mode: Generation of Independent, Periodic Signals, Output in the Up Mode: Edge-Aligned PWM, simple PWM, design of PWM.

UNIT – IV

Mixed signal systems: Comparator_A, Architecture of Comparator_A+, Operation of Comparator_A+, Analog to digital conversion: general issues, Resolution, Precision, and Accuracy, SD 16 sigma delta ADC, signal conditioning and operational amplifiers: Thermistor for range 5°C – 30°C.
UNIT – V

Communication: Communication peripherals in MSP430, serial peripheral interface, SPI with USI, Inter-integrated circuit bus: Hardware for I2C, I2C protocol.

Self Study: Clock generator, driving an LCD from an MSP430x4xx, Basic timer1, real time clock, Architecture of Sigma Delta ADC, Asynchronous serial communication.

Textbook:

Reference:

Course Outcomes:
1. Explain the addressing modes, generation of constants and instruction sets of MSP430 microcontroller. (POs – 1, 3. PSOs – 1, 2)
2. Demonstrate the interfacing of various devices to the input and output pins of MSP430 using Interrupt Service Routines. (POs – 1, 4. PSOs – 1, 2)
3. Generate independent periodic and PWM signals using different modes of MSP430 timer. (POs – 1, 3. PSOs – 1, 2)
4. Design the conversion of analog inputs to digital outputs using comparator A+ and Sigma Delta ADC. (POs – 1, 4. PSOs – 1, 2)
5. Describe communication between peripherals using SPI and I2C. (PO – 1, 3. PSO – 1, 3)
MICROWAVE DEVICES AND RADAR

Course Code: EC63  Credits: 3:0:0:1
Prerequisites: Transmission Lines & Radiating Systems  Contact Hours: 42
Course Coordinator: Mrs. Sujatha B

UNIT – I


UNIT – II

Microwave Passive and Active devices: Composite filter design by the image parameter method, PIN diodes, Phase shifters, Schottky-barrier diode, Attenuator, RWH theory, Gunn diodes– Gunn effect, modes of operation.

UNIT – III

Microwave Tubes: Introduction, Klystrons: Two cavity klystron amplifiers, Multicavity Klystron Amplifiers, Reflex Klystrons: Mathematical analysis of power and efficiency, Traveling Wave Tubes, Magnetron Oscillators.

UNIT – IV


UNIT – V


Self-Study: Impedance, admittance and transmission matrices of reciprocal microwave networks and lossless microwave networks, Stepped-impedance low-pass filters, varactor diode and its applications, IMPATT diode and its applications, conventional vacuum tubes comparison, applications of Klystron amplifier, oscillator, applications of TWTA, applications of magnetron oscillator, origins of radar, applications of radar, Doppler effect, millimeter waves radar.
Textbooks:


References:


Course Outcomes:

1. Apply the properties of scattering parameters to obtain the S-matrix of microwave components and circuits. (POs – 1, 2. PSO – 3)
2. Examine the consequence of various microwave passive & active devices and design the Microwave filters. (POs – 1, 2, 3, 10. PSO – 3)
3. Illustrate the significance of various microwave tubes. (POs – 1, 2, 10. PSO – 3)
4. Interpret the importance of radar and radar range equation. (PO - 1, 2, 10. PSO – 3)
5. Outline the key role played by special types of radar. (PO – 1, 10. PSO – 3)
MINI PROJECT

Course Code: EC64 Credits: 0:0:6:0

Students will commence and complete a technical project under the guidance of a faculty member in the department. The quality of the work will be judged in two presentations, where the panel consists of the guide and at least two other faculty members in the project domain.

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Subject</th>
<th>No. of Hrs/Week</th>
<th>Duration of Exam (Hrs)</th>
<th>Marks</th>
<th>Total Marks</th>
<th>Credits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Lecture</td>
<td>Practical/Field Work</td>
<td>IA</td>
<td>Exam</td>
<td></td>
</tr>
<tr>
<td>EC64</td>
<td>Mini-project</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>50</td>
</tr>
</tbody>
</table>

Course Outcomes:

1. Perform a survey of existing methods in the domain of the chosen topic (POs – 1, 2, 3, 4, PSO – 1)
2. Describe the proposed design in terms of its technical block diagram (POs – 2, 3, 10, PSOs – 2, 3)
3. Implement the technical block diagram using appropriate tools (POs – 2, 3, 4, 5, PSOs – 2, 3)
4. Conduct extensive experimentation to evaluate the quality of the design (POs – 2, 3, 4, 5, PSOs – 2, 3)
5. Present and prepare technical details of the project at regular intervals (POs – 9, 10, PSOs – 2, 3)
## EVALUATION RUBRICS

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Max. Marks</th>
<th>Inadequate (0% – 33%)</th>
<th>Development (34% – 66%)</th>
<th>Proficient (67% – 100%)</th>
<th>Marks</th>
<th>CO Mapping</th>
</tr>
</thead>
<tbody>
<tr>
<td>Introduction to area (Review I)</td>
<td>10</td>
<td>No information about the specific technical details in the chosen area.</td>
<td>Some information about the area, but no clarity in internal details.</td>
<td>Clear presentation of the technical details, internal working, and rationale of design choices.</td>
<td></td>
<td>COs – 1, 5</td>
</tr>
<tr>
<td>Explanation of Technical Block Diagram (Review I)</td>
<td>10</td>
<td>Block diagram is not technically correct, or is not feasible.</td>
<td>Technically correct block diagram, but not practical with existing data/tools/methods.</td>
<td>Technically correct block diagram with ample resources for implementation.</td>
<td></td>
<td>COs – 2, 5</td>
</tr>
<tr>
<td>Implementation of Block Diagram (Review II)</td>
<td>10</td>
<td>Incomplete or no implementation of diagram, using unsuitable tools.</td>
<td>Block diagram is implemented, but results are not matching initial predictions.</td>
<td>Complete implementation using suitable tools, and producing consistent results.</td>
<td></td>
<td>COs – 3, 5</td>
</tr>
<tr>
<td>Results &amp; Discussion (Review II)</td>
<td>10</td>
<td>No or insufficient experimentation to rest working.</td>
<td>Simple experiments to show functionality, without exhausting testing.</td>
<td>Complete experimental analysis including corner cases/weaknesses of design.</td>
<td></td>
<td>COs – 4, 5</td>
</tr>
<tr>
<td>Presentation and Report (Review I, II)</td>
<td>10</td>
<td>No proper use of tables/media, unscientific language in report.</td>
<td>Basic use of media, no continuity/flow in report and presentation.</td>
<td>Media effectively used, along with a smooth flow from beginning to end, scientific language used in report.</td>
<td></td>
<td>CO – 5</td>
</tr>
</tbody>
</table>

**TOTAL MARKS AWARDED**
DIGITAL COMMUNICATION LABORATORY

Course Code: ECL65
 Credits: 0:0:1:0
Prerequisites: Analog Communication
 Contact Sessions: 14
Course Coordinator: Mr. Sadashiva V Chakrasali

LIST OF EXPERIMENTS

1. Verification of sampling theorem
2. Time Division Multiplexing
3. Generation and detection of Amplitude Shift Keying signals
4. Generation and detection of Frequency Shift Keying signals
5. Generation and detection of Phase Shift Keying signals
6. Generation and detection of Quadrature PSK & DPSK
7. PCM modulation and demodulation
8. Delta modulation and demodulation
9. Simulation for verification of sampling theorem
10. Simulation for performance analysis of various digital modulation and demodulation techniques

Textbooks:


Course Outcomes:

1. Implement a sampling circuit to find Nyquist rate. (POs – 1, 2, 3, 5, 6, 8, 11. PSO – 3)
2. Employ TDM for band limited signals. (POs – 1, 2, 11. PSO – 3)
3. Design and implement ASK, PSK, FSK, DPSK digital modulation schemes. (POs – 3, 4, 7, 11. PSO – 3)
4. Design and implement PCM and Delta modulation scheme. (POs – 3, 4, 5, 7, 11. PSO – 3)
5. Analyze the performance of various modulation techniques. (PO – 2, 4, 11. PSO – 3)
MICROWAVE AND ANTENNAS LABORATORY

Course Code: ECL66  
Prerequisite: Transmission Line & Radiating Systems  
Course Coordinator: Mrs. Sujatha B

LIST OF EXPERIMENTS

1. Verify the power division and calculate insertion loss and isolation of a hybrid network (Magic tee).
2. Determination of coupling and isolation characteristics of a microstrip, branch line directional coupler
3. Determination of coupling and isolation characteristics of a microstrip backward directional coupler
4. Measurement of resonance characteristics of a microstrip ring resonator and determination of dielectric constant
5. Measurement of power division and isolation characteristics of a microstrip 3 dB power divider
6. Verify the power division and calculate insertion loss and isolation of a waveguide directional coupler
7. Characteristics of Gunn diode
8. Mode curves of Reflex Klystron
9. Radiation pattern and directivity of Horn antenna
10. Radiation pattern and directivity of Yagi-uda antenna
11. Radiation pattern and directivity of dipole antenna
12. Radiation pattern and directivity of patch antenna

Textbooks:


Course Outcomes:

1. Analyze the characteristics of multiport waveguide microwave networks. (POs – 1, 2, 9, 10. PSO – 3)
2. Interpret the characteristics of microwave oscillators. (POs –1, 2, 9, 10. PSO – 3)
3. Obtain the radiation pattern and calculate the directivity and gain of horn antenna. (POs – 1, 2, 9, 10. PSO – 3)
4. Calculate the parameters of printed antennas (POs – 1, 2, 9, 10. PSO – 3)
5. Analyze the power division in micro-strip microwave network. (POs – 1, 2, 9, 10. PSO – 3)
LIST OF EXPERIMENTS

Part A: Assembly Language Programming

1. Data block move: with overlap, without overlap and interchange
2. Addition, subtraction, multiplication and division of N-bit multi precision numbers (N > 32 bits)
3. Identify whether a given number is positive, negative, odd and even
4. Sorting and Finding smallest/largest element in an array
5. Code conversion between BCD, ASCII & Hexadecimal
6. Square, cube, LCM, HCF and Factorial of a number
7. Addition and subtraction of two string ASCII digits
8. String transfer and string reversal
9. Identify whether a string is palindrome

Part B: Interfacing

Write C programs to interface MSP430 with peripherials:

10. Toggle LEDs using Timer_A to set delay
11. Identify a key press by interfacing keypad with 7 segment display
12. Display on LCD: a key pressed or a message on the LCD module
13. Seven segment interface: 4 digit up/down binary and decimal counter
14. Generating pulse width modulation

Textbook:


Reference:


Course Outcomes:

1. Employ hardware and software development and debugging tool. (PO – 5. PSO – 2)
2. Write, compile and debug assembly language program. (POs – 1, 2, 3, 5. PSO – 2)
3. Develop C programs for different applications. (POs – 1, 2, 4, 5. PSO – 2)
4. Write C language programs to interface modules to MSP430 microcontroller. (POs – 1, 2, 4, 5. PSOs – 2, 3)
5. Write assembly language programs to use GPIO ports and timer module of MSP430 microcontroller. (PO – 10. PSOs – 2)
DEPARTMENT ELECTIVES

POWER ELECTRONICS

Course Code: ECE01
Prerequisites: Analog Electronic Circuits
Course Coordinator/s: Mrs. Punya Prabha. V, Mrs. Reshma Verma

Credits: 3:0:0:1
Contact Hours: 42

UNIT – I

Introduction: Application of power electronics, power semiconductor devices, control characteristics of power devices, types of power electronic circuits, peripheral effects.

Thyristors: Static characteristics, two- transistor model, dynamic characteristics turn on and turn-off

Power MOSFET: Structure, operation, concept of pinch-off, steady state characteristics, switching characteristics, gate drive.

IGBT: Structure of punch-through and non-punch-through IGBT, operation, steady state characteristics, switching characteristics.

UNIT – II

DC Choppers: Principle of step-up and step-down chopper


UNIT – III

Inverters: Principle of operation, performance parameters, single phase half and full bridge inverter with R and RL load


UNIT – IV

Automotive Applications of Power Electronics: Introduction, Present Automotive Electrical Power System, System Environment, Functions Enabled by Power Electronics, Multiplexed
Load Control, and Electromechanical Power Conversion, Dual/High Voltage Automotive Electrical Systems, Electric and Hybrid Electric Vehicles.

UNIT – V

**Non-conventional energy sources:** Photovoltaic cells, wind power, LED light circuits,

**Self Study:** Conduct experiments on Static characteristics of Power MOSFET, IGBT, SCR, RC half-wave and full-wave triggering circuit for a thyristor, SCR firing circuit using synchronized UJT relaxation circuit, Commutation circuits for thyristor – LC circuit and Impulse commutation circuit, Voltage impulse commutated chopper, Series Inverter.

**Textbooks:**


**References:**


**Course Outcomes:**

1. Describe the structure, characteristics and operation of power semiconductor devices like Thyristor, MOSFET and IGBT. (PO – 1, PSO – 2)
2. Analyze detailed operation of Power supplies. (POs – 1, 2, PSO – 2)
3. Illustrate the various operations of UPS. (POs – 2, 3, PSO – 2)
4. Investigate the various automotive applications of power electronics (POs – 2, 3, PSO – 2)
5. Analyze electronic ballast for discharge lamps. (PO – 3, 5, 9, PSO – 2)
RANDOM VARIABLES AND RANDOM PROCESS

Course Code: ECE02
Prerequisites: Engineering Mathematics
Course Coordinator: Mr. Sadashiva V Chakrasali

Credits: 3:0:0:1
Contact Hours: 42

UNIT – I

Introduction: Set theory, definitions, conditional probability, Bayes theorem, combined experiments.

Specific Random Variables: Gaussian random variable, other distributions, density functions and examples, conditional distribution and density functions.

UNIT – II

Operations on one random variable: Introduction, Expectation, moments, functions that give moments, Transformations of random variables, computer generation of one random variable.

Multiple random variables: Introduction, vector random variables, joint distribution and its properties, joint density and its properties, conditional distributions and density functions, statistical independence.

UNIT – III

Multiple random variables: Distribution and density function of sum of random variables, central limit theorem.

Random Processes: Introduction, the random process concept, stationarity and independence, correlation functions, measurement of correlation functions.

UNIT – IV


UNIT – V

Self Study: Probability: Set definitions, set operations, probability introduced through sets, joint and conditional probability, independent events and Bernoulli trials, Random Variable: the random variable concept, distribution function, density function.

Textbook:


References:


Course Outcomes:

1. Solve basic probability and random variable problems. (POs – 1, 2, PSOs – 1, 3)
2. Identify different random variables and their properties. (POs – 1, 2, PSOs – 1, 3)
3. Estimate statistical parameters of different random variables. (POs – 1, 2, PSOs – 1, 3)
4. Classify different random processes. (POs – 1, 2, PSOs – 1, 3)
5. Relate input and output processes of a LTI system. (POs – 1, 2, PSOs – 1, 3)
SPEECH PROCESSING

Course Code: ECE03  
Prerequisites: Digital Signal Processing  
Course Coordinator: Mr. Sadashiva V Chakrasali

Credits: 3:0:0:1  
Contact Hours: 42

UNIT – I

Digital Models for the Speech Signal: The process of speech production, the acoustic theory of speech production, lossless tube models.

UNIT – II

Time Domain Models for Speech Processing: Time dependent processing of speech, short time energy and average magnitude, speech and silence determination, pitch period estimation.

UNIT – III

Digital Representations of the Speech Waveform: Sampling speech signals, Instantaneous quantization and adaptive quantization, delta modulation, differential PCM.

UNIT – IV

Short Time Fourier analysis and Homomorphic speech processing: Design of digital filter banks, spectrographic displays, pitch detection, analysis by synthesis, analysis – synthesis systems.

Homomorphic speech processing: The complex cepstrum of speech, Pitch detection, formant estimation.

UNIT – V

Linear Predictive Coding: Linear predictive coding of speech: basic principles of linear predictive analysis, computation of the gain for the model, solution of the LPC equations, relations between various speech parameters, synthesis of speech from linear predictive parameters.

Self Study: Digital models for speech signals, short time average zero crossing rates, direct digital code conversion, implementation of filter bank summation method using FFT, applications of LPC parameters.

Textbooks:


References:


Course Outcomes:

1. Compare various speech production models. (POs – 2, 3, PSO – 3)
2. Find various speech parameters. (POs – 2, 3, PSO – 3)
3. Represent speech signal in different codes. (POs – 2, 3, 5, PSO – 3)
4. Interpret and analyze speech signals in frequency domain. (POs – 2, 3, PSO – 3)
5. Determine LPC parameters for given speech signal. (POs – 2, 3, 5, PSO – 3)
LOW POWER VLSI DESIGN

Course Code: ECE04
Prerequisites: CMOS VLSI Design
Course Coordinator: Dr. V. Anandi

Credits: 3:0:0:1
Contact Hours: 42

UNIT – I

Power Dissipation in CMOS: Introduction: Need for low power VLSI chips, sources of power consumption, introduction to CMOS inverter power dissipation, low power VLSI design limits, basic principle of low power design.

UNIT – II

Power Optimization: Logical Level Power Optimization: gate reorganization, local restructuring, signal gating, logic encoding, state machine encoding, pre-computation logic

Circuit Level Power Optimization: Transistor and gate sizing, equivalent pin ordering, network restructuring and re-organization, special latches and flip-flops.

UNIT – III

Design of Low Power CMOS Circuits: Reducing power consumption in memories: low power techniques for SRAM, Circuit techniques for reducing power consumption in adders and multipliers.

Special techniques: Power reduction and clock networks, CMOS floating gate, low power bus, delay balancing.

UNIT – IV

Power Estimation: Simulation power analysis: SPICE circuit simulation, Gate level Simulation, Architectural level analysis, Data correlation analysis in DSP systems, Monte-Carlo simulation.

Probabilistic Power analysis: Random signals, probabilistic techniques for signal activity estimation, propagation of static probability in logic circuits, gate level power analysis using transition density.
UNIT – V

Synthesis for Low Power: Behavioral level transforms, algorithm level transforms for low power, architecture driven voltage scaling, power optimization using operation reduction, operation substitution, Bus switching activity.

Self Study: Basic principle of low power design, Signal gating, Network restructuring and reorganization, CMOS floating gates, delay balancing in multipliers, SPICE circuit simulation, Random signals, power optimization using Operation reduction

Textbooks:


References:


Course Outcomes:

1. Identify the sources of power dissipation in CMOS circuits. (POs –1, 2, 4, 9, PSO – 2)
2. Investigate low power design techniques. (POs – 2, 4, 6, PSO – 2)
3. Apply optimization and trade-off techniques that involve power dissipation of digital circuits. (POs – 2, 5, 6, PSO – 2)
4. Perform power analysis using simulation and probabilistic based approaches. (POs – 4, 9, 11, PSO – 2)
5. Analyze and design low-power VLSI circuits using current generation design style and process technology. (POs – 2, 4, 5, 11, PSO – 2)
OBJECT ORIENTED PROGRAMMING WITH C++

Course Code: ECE05  
Prerequisite: Data Structures using C  
Course Coordinator: Dr. K. Indira

Contact Hours: 42

UNIT – I

Introduction: Structure of C++ program: Preprocessor directive, declarations and definitions. Functions: Passing simple function, passing arguments to functions such as variables, reference arguments pointer type, function return data type such as constant, variables, data structures, specifying a class, member functions and member data, nested classes, static data members and member functions, friendly functions.

UNIT – II

Classes and Objects: Definition, class initialization, class constructors, destructors, constructor types, multiple constructor in a class, destructors, inheritance, defining derived classes, different types of inheritance, Virtual base classes, abstract classes, constructors in derived classes, virtual functions and dynamic polymorphism, Pure virtual function.

UNIT – III

Operator Overloading: Overloading using various operators, Overloading using friends, Function Overloading. Templates: Function Templates, Class Templates, Header File and Implementation File of a Class Template

UNIT – IV

Pointers: Pointer data types and Pointer Variables, Dynamic Arrays, Classes and Pointers, Overloading the array index operator.

Standard Template Library: Components of STL, Sequence Container, Iterators and Programming Examples

UNIT – V

Stacks: Implementation of Stacks as Arrays, Linked implementation of Stacks Applications of Stacks.

Queues: Implementation of Queues as Arrays, Linked implementation of Queues

Trees: Basic terminologies of binary trees, Binary Tree Traversal, Binary Search Trees
Self Study: Programs using C++ for the following topics: Introduction to C++ Programming, Data types in C++, Manipulators and Functions, Structures, Recursive function and Class, Nested Member Functions and Arrays, Static variables, Static Member Function, Arrays of objects and objects as Arguments, Friend Functions and Constructors, Inheritance, Multiple Inheritance and Virtual Functions, Stacks Queues, Trees and Hashing.

Textbooks:

References:

Course Outcomes:
1. Illustrate the concept of C++ program by using functions with different arguments. (POs – 1, 2, 3, 5, 12, PSO – 2)
2. Apply the concept of inheritance in solving real world problems. (POs – 2, 3, 5, 12, PSO – 2)
3. Employ overloading concepts to overload built in operators. (POs – 2, 3, 5, 12, PSO – 2)
4. Use pointers for dynamic arrays and linked lists. (POs – 2, 3, 5, 12, PSO – 2)
5. Implement the concept of stack, queues and trees using Standard Template Library. (PO – 2, 3, 5, 12, PSO – 2)
DIGITAL SYSTEM DESIGN USING VERILOG

Course Code: ECE06  Credits: 3:0:0:1
Prerequisite: Digital Electronics  Contact Hours: 42
Course Coordinator: Mrs. Lakshmi Shrinivasan

UNIT – I

Introduction and Methodology: Digital systems and embedded systems, Real world circuits, Models, Design Methodology.

Combinational Basics: Boolean function and Boolean Algebra, Binary coding, Combinational components and circuits.

UNIT – II

Sequential Basics: Counters, Sequential data paths and controls, Clocked synchronous timing methodology, Memories: Concepts, Memory types, Error detection and correction.

UNIT – III

Implementation Fabrics: ICs, PLDs, Interconnections and signal integrity, Processor Basics: Embedded computer organization, Instruction and data.

UNIT – IV

Interfacing with memory and I/O Interfacing: I/O devices, I/O Controllers, Parallel Buses, Serial transmission, I/O software.

UNIT – V

Accelerators: General concepts, Case study: Video edge detection, verifying an accelerator.

Design Methodology: Design optimization, Design for test.


Textbook:

References:


Course Outcomes:

1. Describe the basics of combinational components for building digital systems. (POs – 1, 3, PSOs – 1, 2)
2. Apply the sequential basics and memory concepts to build a specified digital system (POs – 1, 2, 3, PSOs – 1, 2)
3. Implement processors and other digital systems on programmable logic devices. (POs – 1, 2, 3, 4, PSOs – 1, 2)
4. Interface different I/O and memory modules in a system. (POs – 1, 2, 3, PSOs – 1, 2)
5. Illustrate the entire digital system design flow. (PO – 1, 2, 3, PSOs – 1, 2)
DSP ARCHITECTURE AND ALGORITHMS

Course Code: ECE07
Prerequisites: Digital Signal Processing
Course Coordinator: Dr. Maya V. Karki

UNIT – I


Architecture and instruction set of C6x processor: TMS320C6x architecture, functional units, fetch and execute units, pipelining, registers, linear and circular addressing modes, instruction sets

UNIT – II

Software and memory consideration of C6x Processor: Assembler directives, Linear assembly, ASM statements within C, C callable assembly function, timers, interrupts, multichannel buffered serial ports, direct memory access, memory considerations, fixed and floating point format, code improvements, constraints, Programming examples using assembly and linear assembly.

UNIT – III

Implementation of FIR filters: FIR filters, FIR lattice structure, FIR implementation using Fourier series, window functions, Programming example using ASM and C

UNIT – IV

Implementation of IIR filters: Introduction, IIR filter structures, Bilinear transformation, Programming examples based on ASM and C

UNIT – V

Self Study: Assembly code format, Programming examples using assembly and linear assembly, Programming example using ASM on FIR and IIR filtering, Programming example using ASM on FFT

Textbook:


References:


Course Outcomes:

1. Distinguish the computational building blocks, architectural features and instruction sets of TMS320C6x (POs – 1, 2, 3, PSO – 3)
2. Compute the programming examples using assembly and linear assembly (POs – 2, 3, 5, PSO – 3)
3. Demonstrate implementation of FIR filters using ASM and C (POs – 2, 3, 5, PSO – 3)
4. Employ ASM and C code to realize IIR filtering (POs – 2, 3, 5, PSO – 3)
5. Illustrate realization of FFT algorithm with Radix-2 and Radix-4 (POs – 2, 3, 5, PSO – 3)
MICRO ELECTRO MECHANICAL SYSTEMS

Course Code: ECE08
Prerequisites: CMOS VLSI Design
Course Coordinator: Mrs. Lakshmi S

Credits: 3:0:0:1
Contact Hours: 42

UNIT – I

Introduction to MEMS: Historical background of Micro Electro Mechanical Systems, multi-disciplinary aspects, basic technologies, application areas, scaling laws in miniaturization, scaling in geometry, electrostatics, electromagnetics, electricity and heat transfer.

UNIT – II


UNIT – III

Materials and Micromanufacturing: Semiconducting materials, Silicon, Silicon dioxide, Silicon Nitride, Quartz, Poly silicon, Polymers, Materials for wafer processing, Packaging materials Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, Silicon micromachining: surface, bulk, LIGA process.

UNIT – IV

Electrical and Electronics Aspects: Electrostatics, Coupled electro mechanics, stability and Pull-in phenomenon, Practical signal conditioning circuits for microsystems, RF MEMS: Switches, varactors.

UNIT – V

Integration and Packaging of Microelectromechanical Systems: Integration of microelectronics and micro devices at wafer and chip levels, Microelectronic packaging: wire and ball bonding, flip chip, Micro system packaging examples.

Self Study: Feynman’s vision, Smart phone applications, Smart buildings, Wafer bonding process, Tuned filters, Application circuits Based on microcontrollers for pressure sensor, Accelerometer, Testing of Micro sensors, Qualification of MEMS devices.
Textbooks:


References:


Course Outcomes:

1. Recognize the multidisciplinary and scaling aspects of micro systems. (POs – 1, 2, 3, 4, PSOs – 2, 3)
2. Analyze the various transduction mechanisms and applications of MEMS. (POs – 1, 2, 3, 4, PSOs – 2, 3)
3. Describe the various fabrication processes of MEMS devices. (POs – 2, 9, 10, 12, PSOs – 2, 3)
4. Analyze the electronics aspects of MEMS systems. (POs – 1, 2, 3, 4, PSOs – 2, 3)
5. Classify the various packaging methods for MEMS devices. (POs – 2, 3, 4, PSOs – 2, 3)
ARTIFICIAL NEURAL NETWORKS AND FUZZY LOGIC

Course Code: ECE09  Credit: 3:0:0:1
Prerequisites: Digital Signal Processing  Contact Hours: 42
Course Coordinator/s: Mrs. Punya Prabha. V

UNIT – I

Fundamentals of Neural Networks: Biological neurons and their artificial models, Neural Network Architecture: Single Layer, Multi layer Feed Forward Networks, Recurrent Networks, Learning methods, Applications.

UNIT – II


UNIT – III


UNIT – IV

Fuzzy Set Theory: Fuzzy vs crisp sets, crisp sets, Operations on crisp sets, Properties of crisp sets, Partition and Covering, Membership function, Basic fuzzy set operations, Properties of Fuzzy sets, Crisp relations and Fuzzy relations, Applications.

UNIT – V

Self Study: Implementation: Pattern classification using Hebb net and McCulloch –Pitts net, Pattern recognition using Perceptron Networks, Implementation of all fuzzy operations on both discrete and continuous fuzzy sets, Defuzzification, Fuzzy inference system

Textbooks:


References:


Course Outcomes:

1. Describe the relation between real brains and simple artificial neural network models. (POs – 1, 6, 12, PSO – 2)
2. Select different neural network algorithms for suitable applications. (POs – 1, 3, 6, 12, PSO – 2)
3. Identify the main implementation issues for common neural network systems and apply ANN models to data compression and pattern identification (POs – 1, 3, 6, 12, PSO – 2)
4. Apply the rules of fuzzy logic for fuzzy controller. (POs – 2, 4, 6, 12, PSO – 2)
5. Employ fuzzy set operations and defuzzification for a given application. (POs – 1, 2, 4, 6, 12, PSO – 2)
UNIT – I

**Introduction and Fundamentals:** What is Digital Image Processing? Origins, Examples, fundamental steps in Digital Image Processing, Components of an image processing system, Elements of visual perception, Image sensing and acquisition, Image sampling and quantization, some basic relationships between pixels, mathematical tools used in image processing.

UNIT – II

**Intensity Transformations and Spatial Filtering:** Basic intensity transformation functions, Histogram processing, spatial filtering, smoothing spatial filters, sharpening spatial filters.

UNIT – III

**Image Transforms:** Two dimensional orthogonal and unitary transforms, property of unitary transforms, 1D-DFT, 2D-DFT, DCT, Basics of filtering in the frequency domain, image smoothing and image sharpening using frequency domain filters.

UNIT – IV

**Image Segmentation – 1:** Fundamentals, Detection of discontinuities, line detection, Edge detection, Edge linking via Hough Transform, Thresholding, Basics of intensity thresholding, Basic global thresholding, Optimum global thresholding using Otsu’s method.

UNIT – V

**Image Segmentation and Morphological Image Processing:** Region based segmentation: Region growing, splitting and merging, Dilation and Erosion, some basic morphological algorithms, segmentation using morphological watersheds.

**Self Study:** Implement programs for image processing basics, reading and display of image, histogram, image sensing, acquisition and sampling, intensity transformations and filtering, DFT, DCT, and thresholding of images, image segmentation and morphological algorithms.
Textbooks:


References:


Course Outcomes:

1. Analyze general terminology of digital image processing. (POs – 1, 2, 3, 5, PSO – 3)
2. Examine various types of images, intensity transformations and spatial filtering. (POs – 2, 3, 5, PSO – 3)
3. Employ Fourier Transform for image processing in frequency domain. (POs – 1, 2, 3, 5, PSO – 3)
4. Apply segmentation algorithms to detect and link edges in an image. (POs – 3, 5, PSO – 3)
5. Develop morphological algorithms to describe the shape of a region in an image. (POs – 2, 3, 5, PSO – 3)
REAL TIME SYSTEMS

Course Code: ECE11
Prerequisite: Microprocessors
Course Coordinator: Mrs. Lakshmi Shrinivasan

UNIT – I


UNIT – II


UNIT – III


UNIT – IV


UNIT – V


Textbook:


References:


Course Outcomes:

1. Describe the basics of real time systems (POs – 1, 2, PSO – 2)
2. Select appropriate scheduling strategy based on real time application constraints (POs – 3, 4, PSOs – 2, 3)
3. Elaborate the language syntax for real time applications (POs – 2, 3, PSO – 2)
4. Identify suitable RTS development methodology for a given application (POs – 3, 4, PSOs – 2, 3)
5. Apply the knowledge of software design specification to build RTS (POs – 1, 2, 3, 4, PSO – 2)
ADVANCED DIGITAL LOGIC DESIGN

Course Code: ECE12  
Prerequisites: Digital Electronic Circuits  
Course Coordinator: Mrs. A. R. Priyarenjini

Credits: 3:0:0:1  
Contact Hours: 42

UNIT – I


Introduction to CMOS Technology: CMOS operation principles, Characteristic curves of CMOS, CMOS inverter and characteristic curves, Delays in inverters, Buffer Design, Power dissipation in CMOS, CMOS Logic, Stick diagrams and Layout diagrams, Timing concepts

UNIT – II


FSM Design: Mealy and Moore modeling, Adder & Multiplier concepts

UNIT – III

Logic Design using Verilog: Lexical Conventions, Data Types, Modules, Nets, Values, Data Types, Comments, arrays in Verilog, Expressions, Operators, Operands, Arrays, memories, Strings, Delays, parameterized designs, Procedural blocks, Blocking and Non-Blocking assignment, looping, flow Control, Task, Function, Synchronization, Event Simulation, need for verification, basic test bench generation and simulation

UNIT – IV

Principles of RTL Design: Verilog coding concepts, Verilog coding guide lines: Combinational, Sequential, FSM, general guidelines, synthesizable Verilog constructs, sensitivity list, Verilog events, RTL design challenges, clock domain crossing, Verilog modeling of combinational logic, Verilog modeling of sequential logic.
UNIT – V

**Design and simulation of architectural building blocks:** Basic Building blocks, design using Verilog HDL: Arithmetic Components – Multiplier design, Data Integrity – Parity Generation circuits, Control logic – Arbitration, FSM Design, overlapping and non-overlapping Mealy and Moore state machine design

Mini-Project: n bit simple ALU design & verification

**Self Study:** Moore’s law, PMOS & NMOS operation, basic gates, universal gates, NAND & NOR CMOS implementation, Evolution & importance of HDL, Introduction to Verilog, Levels of abstraction, typical design flow, design using Verilog HDL, Arithmetic components – Adder, Subtractor.

**Textbooks:**


**References:**


**Course Outcomes:**

1. Understand the basic VLSI design principles. (POs – 1, 2, 3, 4, PSO – 2)
2. Apply basic digital design principles to complex circuits. (POs – 1, 2, 3, 4, 5, PSO – 1, 2)
3. Employ Verilog HDL for describing digital circuits. (POs – 1, 2, 3, 4, 5, PSO – 2)
4. Create directed test benches, run simulators and analyze/debug. (POs – 1, 2, 3, 4, 5, PSO – 2).
5. Employ FSMs for the design of basic sub circuits and use EDA tools to simulate them. (POs – 1, 2, 3, 4, 5, PSO – 2).
ADVANCED DIGITAL LOGIC VERIFICATION

Course Code: ECE13 Credits: 3:0:0:1
Prerequisites: Advanced Digital Logic Design Contact Hours: 42
Course Coordinator: Mr. S. L. Gangadharaih

UNIT – I

Verification Concepts: Concepts of verification, Test bench generation, Functional verification approaches, Typical verification flow, Stimulus generation, Direct testing.

Coverage: Code coverage and Functional coverage, Coverage plan.

UNIT – II


UNIT – III

System Verilog – Classes: Classes and Objects, Class Variables and Methods, Class Instantiation, Inheritance and Encapsulation, Polymorphism.


UNIT – IV

System Verilog – Assertions and Coverage: Introduction to assertion based verification, Immediate and concurrent assertions

Coverage driven assertion: Motivation, types of coverage, Cover group, Cover point, Cross coverage, Concepts of binning and event sampling.

UNIT – V

Building Test bench: Layered test bench architecture, Introduction to universal verification methodology, Overview of UVM.
**Self Study:** Importance of verification, Stimulus vs verification, Language evolution, Introduction to universal verification methodology, Base classes and simulation phases in UVM and UVM macros, Unified messaging in UVM, UVM environment structure, Connecting DUT – Virtual Interface.

**Tools:** NCVerilog, NCSim, VCSMX for System Verilog

**References:**

1. System Verilog LRM

**Reference Websites:** [www.testbench.in](http://www.testbench.in), [www.asic-world.com](http://www.asic-world.com)

**Online material:** Seer recordings

**Course Outcomes:**

1. Express the principle of HDL verification. (POs – 2, 3, 4, 5, PSO – 2)
2. Apply OOPs concepts in System Verilog. (POs – 2, 3, 4, 5, PSO – 2)
3. Build basic verification environment using System Verilog. (POs – 2, 3, 4, 5, PSO – 2)
4. Generate random stimulus and track functional coverage using System Verilog. (POs – 2, 3, 4, 5, PSO – 2)
5. Appreciate the concepts of layered test bench architecture and its components. (POs – 2, 3, 4, 5, PSO – 2)
LINEAR ALGEBRA

Course Code: ECE14
Prerequisite: Engineering Mathematics
Course Coordinator: Mr. Shreedarshan K

Credits: 3:0:0:1
Contact Hours: 42

UNIT – I


UNIT – II

Vector Spaces: Vector Spaces and Subspaces, Null Spaces, Column Spaces and Linear Transformations, Linearly Independent sets, Bases, Co-ordinate Systems, The Dimension of a Vector Space, Rank,..

UNIT – III

Eigen Values and Eigen Vectors: The Characteristic equation, Diagonalization, Eigen Vectors and Linear Transformations.

UNIT – IV


UNIT – V

Symmetric Matrices and Quadratic Forms: Diagonalization of Symmetric Matrices, Quadratic Forms, Singular Value Decomposition.

Self Study: Linear models in engineering, Applications to difference equations, Inner Product, Length and Orthogonality, Constrained Optimization.

Textbooks:

References:


Course Outcomes:

1. Solve systems of linear equations using multiple methods, including Gaussian elimination, matrix inversion and matrix operations. (POs – 1, 2, 3, PSO – 3)
2. Demonstrate understanding of the concepts of vector space and subspace. (POs – 2, 3, 5, PSO – 3)
3. Demonstrate understanding of linear independence, span and basis. (POs – 2, 3, 5, PSO – 3)
4. Determine eigen values and eigenvectors and solve eigen value problems. (POs – 2, 3, 5, PSO – 3)
5. Apply principles of matrix algebra to linear transformations. (POs – 2, 3, 5, PSO – 3)
UNIT – I

Introduction: Probability theory, what is machine learning, example machine learning applications

Supervised Learning: Learning a class from examples, VC dimension, PAC learning, Noise, Learning multiple classes, Regression, Model selection and generalization

UNIT – II

Bayesian Learning: Classification, losses and risks, utility theory MLE, Evaluating an estimator, Bayes estimator, parametric classification

Discriminant functions: Introduction, Discriminant functions, Least squares classification, Fisher’s linear discriminant, fixed basis functions, logistic regression

UNIT – III

Multivariate methods: Multivariate data, Parameter Estimation, Estimation of Missing Values, Multivariate Normal Distribution, Multivariate Classification, Tuning Complexity, Discrete Features, Multivariate Regression

Non-parametric methods: Nearest Neighbor Classifier, Nonparametric Density Estimation

UNIT – IV

Maximum margin classifiers: SVM, Introduction to kernel methods, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression

Mixture models and EM: K – means clustering, Mixture of Gaussians, Hierarchical Clustering, Choosing the Number of Clusters

UNIT – V

Dimensionality reduction: Combining Models
Self Study: Implementation of Histograms, Covariance matrices, Regression with sampling, Bayes classifier, Perceptron algorithm and clustering algorithms

Textbooks:


Course Outcomes:

1. Appreciate the concepts and issues of various learning systems. (POs – 1, 2, 3, 4, PSOs – 1, 3)
2. Employ Bayesian learning and discriminant functions for classification. (POs – 1, 2, 3, 4, PSOs – 1, 3)
3. Evaluate multi-variate and non-parametric methods for regression and classification. (POs – 1, 2, 3, 4, PSOs – 1, 3)
4. Describe maximum margin classifiers and mixture models. (POs – 1, 2, 3, 4, PSOs – 1, 3)
5. Examine various dimensionality reduction algorithms. (POs – 1, 2, 3, 4, PSOs – 1, 3)
ANALOG AND MIXED SIGNAL VLSI DESIGN

Course Code: ECE16
Prerequisite: CMOS VLSI Design
Course Credits: 3:0:0:1
Contact Hours: 42
Course Coordinator: Dr. M Nagabhushan

UNIT – I

Single Stage Amplifiers: Common Source stage with different loads and source degeneration, Source follower, Common Gate stage, Cascode structures and Folded Cascode structures.

UNIT – II


UNIT – III


UNIT – IV


UNIT – V

Data Converters: Analog vs Digital and Discrete time signals, converting analog signals to digital signals, Sample and Hold characteristics, DAC Specifications, ADC Specifications, DAC Architectures, Digital input code, Resistor String, R – 2R Ladder Networks, Current steering, Charge scaling DACs, Cyclic DAC, Pipeline DAC, ADC Architectures. Flash type, 2-Step Flash, Pipeline ADC, Integrating ADC, Successive Approximation methods.

Self Study: Differential amplifiers with different loads, Op-amp low frequency analysis, frequency response of cascode structures, ADC & DAC specifications, cyclic DAC
Textbooks:


References:


Course Outcomes:

1. Appreciate the basic concepts of single amplifier design and cascode Amplifier. (POs – 1, 2, 3, 4, 6, 10, 11, PSOs – 1, 2)
2. Design a multistage amplifier using single stage amplifier concept. (POs – 2, 3, 4, 6, 10, 11, PSOs – 1, 2)
3. Determine the poles and zeroes of a multi-pole system and analyze the frequency response and stability of the system. (POs – 2, 3, 4, 6, 11, PSOs – 1, 2)
4. Design an operational amplifier to optimize its performance metrics. (POs – 1, 2, 3, 4, 6, 8, 10, 11, PSO – 1, 2)
5. Analyze different ADC/DAC architectures. (POs – 1, 2, 3, 4, 6, 8, 10, 11, PSOs – 1, 2)
NEURAL NETWORKS AND DEEP LEARNING

Course Code: ECE17  Credits: 3:0:0:1
Prerequisites: Machine Learning  Contact Hours: 42
Course Coordinator: Dr. S. Sethu Selvi

UNIT – I

Introduction: Human brain, neuron models, neural nets as directed graphs, feedback, neural architectures, knowledge representation, connection to artificial intelligence

UNIT – II

Learning process: Error-correction learning, memory based learning, Hebbian learning, competitive learning, Boltzmann learning, credit assignment, learning with and without a teacher, learning tasks, memory, statistical learning theory

UNIT – III

Modern practical deep neural networks: Deep feed forward networks, regularization for deep learning, optimization for training deep models, convolutional networks

UNIT – IV

Sequence Modeling: Recurrent and Recursive nets, Practical Methodology, applications

UNIT – V

Deep Learning Research: Linear factor models, auto encoders, variational auto encoders, restricted Boltzmann machine, generative adversarial networks

Self Study: Implementation of neural network and deep learning algorithms

Textbooks:


Course Outcomes:

1. Appreciate the concepts and applications of neural networks and deep learning (POs – 2, 3, 4, 5, PSOs – 1, 3)
2. Examine how various types of learning work and how they can be used (POs – 2, 3, 4, 5, PSOs – 1, 3)
3. Apply deep feed forward and convolutional networks to solve practical problems (POs – 2, 3, 4, 5, PSOs – 1, 3)
4. Demonstrate how recurrent and recursive nets function and how practical problems can be mapped to them (POs – 2, 3, 4, 5, PSOs – 1, 3)

5. Design end-to-end deep learning architectures involving auto encoders, RBM, and generative adversarial networks for practical applications (POs – 2, 3, 4, 5, PSOs – 1, 3)